PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 14 January 2000 (14.01.00)	
International application No. PCT/DK99/00323	**Applicant's or agent's file reference** 23055 PC 1
International filing date (day/month/year) 11 June 1999 (11.06.99)	**Priority date** (day/month/year) 11 June 1998 (11.06.98)
Applicant VISCOR, Petr et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

03 December 1999 (03.12.99)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer A. Karkachi
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

09/700463

PCT

REQUEST

Received with thanks
11 JUNI 1999
PLOUGMANN VINGTOFT & PARTNERS

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference *(if desired) (12 characters maximum)* 23055 PC 1

Box No. I TITLE OF INVENTION

Planar electron emitter (PEE)

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

VISCOR, Petr
Skjoldenæsvej 17
DK-4174 Jystrup

[X] This person is also inventor.

Telephone No.

Facsimile No.

Teleprinter No.

State *(that is, country)* of nationality: Slovakia

State *(that is, country)* of residence: Denmark

This person is applicant for the purposes of: [X] all designated States [ ] all designated States except the United States of America [ ] the United States of America only [ ] the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

NIELSEN, Niels Ole
Zeltnersvej 7
DK-8600 Silkeborg

This person is:

[ ] applicant only

[X] applicant and inventor

[ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: Denmark

State *(that is, country)* of residence: Denmark

This person is applicant for the purposes of: [X] all designated States [ ] all designated States except the United States of America [ ] the United States of America only [ ] the States indicated in the Supplemental Box

[X] Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: [X] agent [ ] common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

Plougmann, Vingtoft & Partners A/S
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Teleprinter No.

[ ] **Address for correspondence:** Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Continuation of Box No. III **FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)**

If none of the following sub-boxes is used, this sheet should not be included in the request.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

DELONG, Armin
Kalvodova 25
60200 Brno
Czech Republic

This person is:
- [ ] applicant only
- [X] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: Czech Republic

State *(that is, country)* of residence: Czech Republic

This person is applicant for the purposes of:
- [X] all designated States
- [ ] all designated States except the United States of America
- [ ] the United States of America only
- [ ] the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

KOLARIK, Vladimir
Jecna 32
62100 Brno
Czech Republic

This person is:
- [ ] applicant only
- [X] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: Czech Republic

State *(that is, country)* of residence: Czech Republic

This person is applicant for the purposes of:
- [X] all designated States
- [ ] all designated States except the United States of America
- [ ] the United States of America only
- [ ] the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

This person is:
- [ ] applicant only
- [ ] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality:

State *(that is, country)* of residence:

This person is applicant for the purposes of:
- [ ] all designated States
- [ ] all designated States except the United States of America
- [ ] the United States of America only
- [ ] the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

This person is:
- [ ] applicant only
- [ ] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality:

State *(that is, country)* of residence:

This person is applicant for the purposes of:
- [ ] all designated States
- [ ] all designated States except the United States of America
- [ ] the United States of America only
- [ ] the States indicated in the Supplemental Box

- [ ] Further applicants and/or (further) inventors are indicated on another continuation sheet.

Box No.V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked)*:

Regional Patent

- ☒ AP **ARIPO Patent:** GH Ghana, GM Gambia, KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SZ Swaziland, UG Uganda, ZW Zimbabwe, and any other State which is a Contracting State of the Harare Protocol and of the PCT
- ☒ EA **Eurasian Patent:** AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakhstan, MD Republic of Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- ☒ EP **European Patent:** AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, CY Cyprus, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT
- ☒ OA **OAPI Patent:** BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, GW Guinea-Bissau, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)* .....

National Patent *(if other kind of protection or treatment desired, specify on dotted line)*:

- ☒ AL Albania .....
- ☒ AM Armenia .....
- ☒ AT Austria and utility model
- ☒ AU Australia .....
- ☒ AZ Azerbaijan
- ☒ BA Bosnia and Herzegovina .....
- ☒ BB Barbados
- ☒ BG Bulgaria .....
- ☒ BR Brazil .....
- ☒ BY Belarus .....
- ☒ CA Canada
- ☒ CH and LI Switzerland and Liechtenstein
- ☒ CN China .....
- ☒ CU Cuba .....
- ☒ CZ Czech Republic and utility model
- ☒ DE Germany and utility model
- ☒ DK Denmark and utility model
- ☒ EE Estonia and utility model
- ☒ ES Spain .....
- ☒ FI Finland and utility model
- ☒ GB United Kingdom
- ☒ GD Grenada
- ☒ GE Georgia .....
- ☒ GH Ghana .....
- ☒ GM Gambia
- ☒ HR Croatia .....
- ☒ HU Hungary .....
- ☒ ID Indonesia
- ☒ IL Israel .....
- ☒ IN India .....
- ☒ IS Iceland
- ☒ JP Japan .....
- ☒ KE Kenya .....
- ☒ KG Kyrgyzstan .....
- ☒ KP Democratic People's Republic of Korea .....
- ☒ KR Republic of Korea .....
- ☒ KZ Kazakhstan .....
- ☒ LC Saint Lucia
- ☒ LK Sri Lanka
- ☒ LR Liberia
- ☒ LS Lesotho .....
- ☒ LT Lithuania
- ☒ LU Luxembourg
- ☒ LV Latvia
- ☒ MD Republic of Moldova .....
- ☒ MG Madagascar .....
- ☒ MK The former Yugoslav Republic of Macedonia .....
- ☒ MN Mongolia
- ☒ MW Malawi .....
- ☒ MX Mexico .....
- ☒ NO Norway
- ☒ NZ New Zealand .....
- ☒ PL Poland .....
- ☒ PT Portugal .....
- ☒ RO Romania
- ☒ RU Russian Federation .....
- ☒ SD Sudan
- ☒ SE Sweden
- ☒ SG Singapore
- ☒ SI Slovenia .....
- ☒ SK Slovakia and utility model
- ☒ SL Sierra Leone
- ☒ TJ Tajikistan .....
- ☒ TM Turkmenistan .....
- ☒ TR Turkey .....
- ☒ TT Trinidad and Tobago .....
- ☒ UA Ukraine .....
- ☒ UG Uganda .....
- ☒ US United States of America .....
- ☒ UZ Uzbekistan .....
- ☒ VN Viet Nam .....
- ☒ YU Yugoslavia .....
- ☒ ZW Zimbabwe .....

Check-boxes reserved for designating States (for the purposes of a national patent) which have become party to the PCT after issuance of this sheet:

- ☐ AE United Arab Emirates .....
- ☐ ZA South Africa .....
- ☐ .....

Precautionary Designation Statement: In addition to the designations made above, the applicant also makes under Rule 4.9(b) all other designations which would be permitted under the PCT except any designation(s) indicated in the Supplemental Box as being excluded from the scope of this statement. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation of a designation consists of the filing of a notice specifying that designation and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.)*

Box No. VI PRIORITY CLAIM ☐ Further priority claims are indicated in the Supplemental Box.

Filing date of earlier application (day/month/year)	Number of earlier application	Where earlier application is: national application: country	regional application:* regional Office	international application: receiving Office
item (1) 11 June 1998 (11.06.98)	60/088,978	US		
item (2)				
item (3)				

☐ The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) *(only if the earlier application was filed with the Office which for the purposes of the present international application is the receiving Office)* identified above as item(s): _____

* *Where the earlier application is an ARIPO application, it is mandatory to indicate in the Supplemental Box at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed (Rule 4.10(b)(ii)). See Supplemental Box.*

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(if two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used)*:

ISA / EP

Request to use results of earlier search; reference to that search *(if an earlier search has been carried out by or requested from the International Searching Authority)*:

Date *(day/month/year)* Number Country *(or regional Office)*

Box No. VIII CHECK LIST; LANGUAGE OF FILING

This international application contains the following **number of sheets**:

request	: 4
description (excluding sequence listing part)	: 48
claims	: 12
abstract	: 1
drawings	: 24
sequence listing part of description	:
Total number of sheets	: 89

This international application is **accompanied** by the item(s) marked below:

1. ☒ fee calculation sheet
2. ☐ separate signed power of attorney
3. ☐ copy of general power of attorney; reference number, if any:
4. ☐ statement explaining lack of signature
5. ☒ priority document(s) identified in Box No. VI as item(s): (1)
6. ☐ translation of international application into (language):
7. ☐ separate indications concerning deposited microorganism or other biological material
8. ☐ nucleotide and/or amino acid sequence listing in computer readable form
9. ☐ other *(specify)*:

Figure of the drawings which should accompany the abstract:

Language of filing of the international application:

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).

Copenhagen, 11 June 1999

Plogmann, Vingtoft & Partners A/S

Steen Madsen

For receiving Office use only

1. Date of actual receipt of the purpc international application:
2. Drawings: ☐ received: ☐ not received:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:
4. Date of timely receipt of the required corrections under PCT Article 11(2):
5. International Searching Authority (if two or more are competent): ISA /
6. ☐ Transmittal of search copy delayed until search fee is paid.

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/DK 99/00323

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01J1/30 H01L29/76

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01J H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 1 223 729 A (NORTH AMERICAN ROCKWELL CORPORATION) 3 March 1971 (1971-03-03) page 3, line 124 - page 4, line 10 page 4, line 78 - line 77 page 4, line 110 - line 118 page 5, line 14 - line 22 page 7, line 54 - line 112 figures 2,3	1,6-10, 12,13, 18-23, 25,53, 58-62,64
Y	---	34-41, 46-52
Y	US 5 280 221 A (OKAMOTO SHINJI ET AL) 18 January 1994 (1994-01-18) figures 2A-2B	34-40

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 September 1999	28/09/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Colvin, G

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/DK 99/00323

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	DELONG A ET AL: "A 1:1 ELECTRON STEPPER" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 7, no. 6, 1 November 1989 (1989-11-01), pages 1422-1425, XP000117170 ISSN: 0734-211X the whole document	41,46-52
X	EP 0 367 195 A (MATSUSHITA ELECTRIC IND CO LTD) 9 May 1990 (1990-05-09) column 6, line 22 - line 30 column 15, line 51 - column 16, line 5 column 16, line 16 - line 40	1,13,41, 53
A	L F EASTMAN ET AL.: "Ballistic electron motion in GaAs at room temperature" ELECTRONICS LETTERS., vol. 16, no. 13, 19 June 1980 (1980-06-19), pages 524-525, XP002115049 IEE STEVENAGE., GB ISSN: 0013-5194 the whole document	2,14,26, 42,54

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/DK 99/00323

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 1223729 A	03-03-1971	BE 716262 A	04-11-1968
		FR 1572047 A	20-06-1969
US 5280221 A	18-01-1994	JP 4312738 A	04-11-1992
		FR 2675306 A	16-10-1992
EP 0367195 A	09-05-1990	JP 2121227 A	09-05-1990
		JP 2126531 A	15-05-1990
		JP 2126532 A	15-05-1990
		JP 2170327 A	02-07-1990
		JP 2172127 A	03-07-1990
		US 5202605 A	13-04-1993

CLAIMS

1. An article comprising

- an element having a first and a second surface, wherein

  - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, the first surface being substantially parallel to the second surface, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- means for providing an electric field across at least part of the element, said means comprising

  - means for providing the first electrical charge to the first surface of the element, and

  - means for providing the second electrical charge to the second surface of the element, the second electrical charge being different from the first electrical charge in order to move electrons in a direction substantially perpendicular to the first or the second surface.

2. An article according to claim 1, wherein the material or material system comprises a semiconductor material, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

3. An article according to claim 1 or 2, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

4. An article according to claim 3, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

5. An article according to claim 3, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

6. An article according to any of claims 1-5, wherein the means for providing the first electrical charge to the first surface comprises an at least partly conductive first material or material system.

7. An article according to any of claims 1-5, wherein the means for providing the second electrical charge to the second surface comprises an at least partly conductive second material or material system.

8. An article according to claim 6, wherein the at least partly conductive first material or material system constitutes a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element.

9. An article according to claim 7, wherein the at least partly conductive second material or material system constitutes a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

10. An article according to any of claims 6-9, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor material with a doping level higher than $1x10^{17}$ cm^{-3}.

11. An article according to claim 10, wherein the at least partly conductive first and second material or material system comprises gold, chromium, platinum, aluminium, copper, cesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

12. An article according to any of claims 1-11, wherein the electrons comprise quasi-ballistic electrons.

13. A method for providing a first type of electrons, said method comprising the steps of:

- providing an element having a first and a second surface, wherein

  - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, the first surface being substantially parallel to the second surface, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- providing means for providing the first electrical charge to the first surface of the element, and

- providing means for providing the second electrical charge to the second surface of the element, the second electrical charge being different from the first electrical charge so as to move a second type of electrons in a direction substantially perpendicular to the first or second surface.

14. A method according to claim 13, wherein the material or material system comprises a semiconductor material, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

15. A method according to claim 13 or 14, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

16. A method according to claim 15, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

17. A method according to claim 15, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

18. A method according to any of claims 13-17, wherein the means for providing the first electrical charge to the first surface comprises an at least partly conductive first material or material system.

19. A method according to any of claims 13-17, wherein the means for providing the second electrical charge to the second surface comprises an at least partly conductive second material or material system.

20. A method according to claim 18, wherein the at least partly conductive first material or material system constitutes a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element.

21. A method according to claim 19, wherein the at least partly conductive second material or material system constitutes a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

22. A method according to claim 20 or 21, wherein a potential difference between the first and second terminals of the charge reservoir is larger than 2 volts.

23. A method according to any of claims 18-21, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor material with a doping level higher than $1x10^{17}$ cm^{-3}.

24. A method according to claim 23, wherein the at least partly conductive first and second material or material system comprises gold, chromium, platinum, aluminium, copper, cesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

25. A method according to any of claims 13-24, wherein the second type of electrons comprises quasi-ballistic electrons.

26. A method for fabricating an article, said method comprising the steps of:

- providing a semiconductor material or material system having a first and a second surface, the second surface being substantially parallel to the first surface, the semiconductor material or material system having a predetermined crystal orientation perpendicular to the first or second surface,

- providing a surface treatment to the first and second surfaces so as to reduce surface roughness,

- doping the semiconductor material or material system with a dopant so as to obtain a predetermined doping level so as to reduce electron scattering within the material or material system,

- providing an at least partly conductive first material or material system, said first material or material system forming a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element, and

- providing an at least partly conductive second material or material system, said second material or material system forming a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

27. A method according to claim 26, wherein the semiconductor material comprises silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

28. A method according to claim 26 or 27, wherein the predetermined crystal orientation is the <111>, <110> or <100> direction.

29. A method according to any of claims 26-28, wherein the surface treatment comprising optical polishing.

30. A method according to any of claims 26-29, wherein the dopant comprises lithium, phosphorus, antimony, arsenic, boron, aluminium, tantalum, gallium or indium or any combination thereof.

31. A method according to any of claims 26-30, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

32. A method according to any of claims 26-31, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor material with a doping level larger than $1x10^{17}$ cm^{-3}.

33. A method according to claim 32, wherein the at least partly conductive first and second material or material system comprises gold, platinum, chromium, aluminium or copper or any combination thereof.

34. A flat panel display comprising

- an article according to any of claims 1-12, the article further comprising

- a layer of material being adapted to emit light at a plurality of wavelengths upon exposure of electrons, said material layer defining, in a plane substantially parallel to the first and second surface of the element, a two-dimensional matrix having one or more surface elements, each surface element being adapted to emit light at a predetermined wavelength, and

- means for selectively proving electrons to the one or more surface elements in the two-dimensional matrix.

35. A flat panel display according to claim 34, wherein the material layer for emitting the plurality of wavelengths comprise an appropriate luminophors or standard colour television phosphors.

36. A flat panel display according to claim 34 or 35, wherein the emitted light comprises at least three wavelengths corresponding to at least three colours.

37. A flat panel display according to claim 36, wherein any colour may be deduced from a combination of the at least three colours emitted from the layer.

38. A flat panel display according to any of claims 34-37, wherein the emitted wavelengths corresponds to colours red, yellow and blue, or to colours red, green and blue.

39. A flat panel display according to any of claims 34-38, wherein the electrons comprise quasi-ballistic electrons.

40. A flat panel display according to any of claims 34-39, wherein the selective means comprises a pattern so as to define, in a plane substantially parallel to the first or second surface, a two-dimensional matrix of electrically controllable matrix

elements, said pattern being formed of the at least partly conductive material or material system.

41. A method for exposing a film to a plurality of electrons of a first type, said method comprising the steps of:

- providing a first element having a first and a second surface, wherein

  - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- providing a second element, said second element being adapted to hold the film to be exposed to the plurality of electrons of the first type,

- providing a patterned absorption layer, said absorption layer being adapted to absorb electrons transmitted through the first element at positions determined by the pattern,

- providing the first electrical charge to the first surface of the first element, and

- providing the second electrical charge to the second surface of the first element, the second electrical charge being of opposite sign compared to the first electrical charge so as to move a second type of electrons from the first surface towards the second surface, and

- providing a third electrical charge to the second element, said third electrical charge having the same sign as the second electrical charge.

42. A method according to claim 41, wherein the material or material system

comprises a semiconductor material, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

43. A method according to claim 41 or 42, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

44. A method according to claim 43, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

45. A method according to claim 43, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

46. A method according to any of claims 41-45, wherein the first electrical charge is provided to the first surface of the first element from a first terminal of a charge reservoir.

47. A method according to any of claims 41-45, wherein the second electrical charge is provided to the second surface of the first element from a second terminal of the charge reservoir.

48. A method according to any of claims 41-44, wherein the third electrical charge is provided to the second element from a third terminal of the charge reservoir.

49. A method according to claim 46 or 47, wherein a potential difference between the first and second terminals of the charge reservoir is larger than 2 volts.

50. A method according to any of claims 41-49, wherein the second element comprises a metal or a semiconductor material, such as silicon, germanium, silicon

carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

51. A method according to any of claims 41-50, wherein the film comprises a resist.

52. A method according to any of claims 41-51, wherein the second type of electrons comprises quasi-ballistic electrons.

53. An article comprising

- an element having a first and a second surface area, wherein

    - the first surface area is adapted to hold a first electrical charge, and wherein the second surface area is adapted to hold a second electrical charge, and wherein

    - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- means for providing an electric field across at least part of the element, said means comprising

    - means for providing the first electrical charge to the first surface area of the element, and

    - means for providing the second electrical charge to the second surface area of the element, the second electrical charge being different from the first electrical charge in order to move electrons between the first surface area and the second surface area.

54. An article according to claim 53, wherein the material or material system comprises a semiconductor material, such as silicon, germanium, silicon carbide,

gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

55. An article according to claim 53 or 54, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

56. An article according to claim 55, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

57. An article according to claim 55, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

58. An article according to any of claims 53-57, wherein the means for providing the first electrical charge to the first surface comprises an at least partly conductive first material or material system.

59. An article according to any of claims 53-57, wherein the means for providing the second electrical charge to the second surface comprises an at least partly conductive second material or material system.

60. An article according to claim 58, wherein the at least partly conductive first material or material system constitutes a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element.

61. An article according to claim 59, wherein the at least partly conductive second material or material system constitutes a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge

reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

62. An article according to any of claims 57-60, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor with a doping level higher than $1x10^{17}$ cm^{-3}.

63. An article according to claim 61, wherein the at least partly conductive first and second material or material system comprises gold, chromium, platinum, aluminium, copper, cesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

64. An article according to any of claims 53-63, wherein the electrons comprise quasi-ballistic electrons.

PATENT COOPERATION TREATY 09/700463

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

15

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
23055 PC 1		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/DK99/00323	11/06/1999	11/06/1998
International Patent Classification (IPC) or national classification and IPC H01J1/30		
Applicant VISCOR, Petr et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 9 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
03/12/1999	27.09.2000
Name and mailing address of the international preliminary examining authority: European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	Authorized officer Colvin, G Telephone No. +31 70 340 2864

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/DK99/00323

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-48 as originally filed

Claims, No.:

1-4,6-51 as received on 17/07/2000 with letter of 17/07/2000

Drawings, sheets:

1/24-24/24 as originally filed

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-4,6-51
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-4,6-51
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-4,6-51
	No:	Claims	

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following document:

D1: GB-A-1 223 729 [North American Rockwell Corporation]

2.1 Document D1, which is considered to represent the most relevant state of the art, discloses an electron conducting device according to claim 1 comprising (see fig.2, page 4):

a- an element having first and second surfaces, said surfaces adapted to hold first and second charges;
b- a means for providing an electric field across at least part of the element providing first and second charges to the element, said charges being different from one another and being able to move electrons through the element in a direction perpendicular to the first or second surface.

2.2 The subject-matter of claim 1 differs from D1 in that:

A- the material layer is prepared to reduce electron scattering by being single crystal material with a predetermined crystal orientation perpendicular to the first or second surface;
B- having an impurity concentration less than 10^{14} cm^{-3};
C- the material layer having a thickness greater than 0.2 µm.

In view of the above technical features being absent from D1, it is apparent that the subject-matter of claim 1 is novel (Article 33(2) PCT).

2.3 The problem to be solved by the present invention may therefore be regarded as how to achieve improved electron transport at low voltages. By employing the solution of 2.2 above, so-called quasi-ballistic electron transport in the material layer is made possible. Although D1 discloses quasi-ballistic electron transport, this physical process only takes place in the electron escape surface of the

device. No accelerating electric field is applied across this layer. On the contrary, the dielectric layer of D1 across which an accelerating potential is applied is of a thickness (0.02µm - see page 6, line 86) whereby quantum tunnelling may occur. D1 thus teaches away from thicker layers.

2.4 The solution of the present invention is not made obvious by the known prior art, hence the subject-matter of claim 1 is also inventive (Article 33(3) PCT).

2.5 The subject-matter of claims 2-4, 6-13 are dependent upon claim 1 and merely add additional technical features thereto. The subject-matter of these claims is also novel and inventive.

2.6 Claim 14 discloses an electron emitting device according to any of claims 1-4,6-13. The subject-matter of this claim is also therefore novel and inventive.

2.7 The subject-matter of claim 15 is dependent upon claim 14 and merely add additional technical features thereto. The subject-matter of this claims is therefore novel and inventive.

2.8 Independent claim 16 discloses a process for transporting electrons corresponding to the technical features of claim 1. The subject-mater of this claim is therefore both novel and inventive.

2.9 The subject-matter of claims 17-28 are dependent upon claim 16 and merely add additional process steps thereto. The subject-matter of these claims is also novel and inventive.

2.10 Independent claim 29 discloses a process for fabricating an electron conducting device corresponding to the technical features of claim 1. The subject-mater of this claim is therefore both novel and inventive.

2.11 The subject-matter of claims 30-37 are dependent upon claim 29 and merely add additional process steps thereto. The subject-matter of these claims is also novel and inventive.

2.12 Claim 38 discloses a panel display comprising an electron emitter according to claims 14 or 15. Hence the subject-matter of this claim is also novel and inventive.

2.13 The subject-matter of claims 39-44 are dependent upon claim 38 and merely add additional technical features thereto. The subject-matter of these claims is also novel and inventive.

2.14 Claim 45 discloses a process for exposing a film to electrons comprising the steps of providing an electron emitter according to claims 14 or 15. The subject-mater of this claim is therefore both novel and inventive.

2.15 The subject-matter of claims 46-51 are dependent upon claim 45 and merely add additional process steps thereto. The subject-matter of these claims is also novel and inventive.

Re Item VII

Certain defects in the international application

1 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the document D1 is not mentioned in the description, nor is this documents identified therein.

2 The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

3 The units of measure (Å) employed in the application are not additionally expressed in terms of the units stipulated by Rule 10.1(a) PCT.

Re Item VIII

Certain observations on the international application

1 The embodiment of the invention described on page 39 and shown in figure 19 does not fall within the scope of all the independent claims. This inconsistency between the claims and the description leads to doubt concerning the matter for which protection is sought, thereby rendering the claims unclear (Article 6 PCT).

PATENT COOPERATION TREATY

09/700463

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
23055 PC 1		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/DK 99/00323	11/06/1999	11/06/1998
Applicant		
VISCOR, Petr et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [ ] the text is approved as submitted by the applicant.

   [X] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 3

   [ ] as suggested by the applicant.

   [X] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

The abstract is modified as follows :

Line 15 : add :
said semiconductor or insulator body comprises a material or material system having a predetermined crystal orientation.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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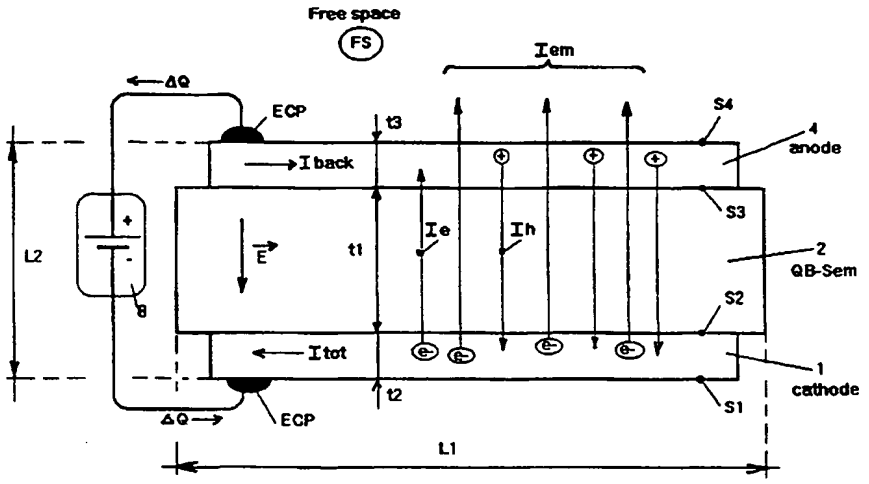
Published
With international search report.

(54) Title: PLANAR ELECTRON EMITTER (PEE)



(57) Abstract

A planar electron emitter, based on the existence of quasi–ballistic transport of electrons is disclosed. In its preferred embodiment the planar electron emitter structure consists of a body of finite gap pure semiconductor or insulator, the said body of macroscopic thickness (~ 1mm) being terminated by two parallel surfaces and of a set of two electrodes deposited/grown on the said two free surfaces such that when a low external electrical field (~ 100V/cm) is applied to this structure, consisting of two electrodes and the said semiconductor or insulating body sandwiched between them, a large fraction of electrons injected into the said semiconductor or insulator body from the negatively charged electrode (cathode) is quasi–ballistic in nature, that is this fraction of injected electrons is accelerated within the said semiconductor or insulator body without suffering any appreciable inelastic energy losses, thereby achieving sufficient energy and appropriate momentum at the positively charged electrode (anode) to be able to traverse through the said anode and to escape from the said structure into empty space (vacuum), said semiconductor or insulator body comprises a material or material system having a predetermined crystal orientation.

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Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

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PLANAR ELECTRON EMITTER (PEE)

FIELD OF THE INVENTION

The present invention relates to a new way to use semiconductor or insulator substrates for creating and conducting quasi-ballistic electrons when exposed to small electric fields. This will make it possible to accelerate electrons within the said semiconductor or insulator body without suffering any appreciable inelastic energy losses. The primary embodiments will be planar electron emitters such as in flat panel displays and Planar Electron Beam Lithography.

A number of apparatuses, using the said (disclosed) planar electron emitter in various fields of application, are also disclosed and the priority rights for the said apparatuses are also claimed.

BACKGROUND OF THE INVENTION

The present invention concerns quasi-ballistic transport of electrons in high resistivity semiconductors or insulators, when exposed to small (around 100 V/cm) electric fields. Quasi-ballistic transport means that electron scattering is reduced to a minimum so that the electron mean free path becomes macroscopic. This effect has so far only been detected in semiconductors when very large electric field strengths are applied over very short distances and/or the semiconductor is cooled down to very low temperatures. A semiconductor or insulator material with the above properties will hereafter be mentioned Quasi-Ballistic Semiconductor or QB-Sem.

The quasi-ballistic transport can be utilised in a number of ways. In this application these will be separated into two major fields:

1. Electron transmitting semiconductors, where it is the transport properties of the quasi-ballistic electrons inside the material which are the characteristic property, and
2. Electron sources, where it is the property of quasi-ballistic electrons to be emitted from the substrate which are the characteristic property.

None of the relevant prior art mentions ballistic electrons in highly resistive semiconductors or insulators, neither when exposed to large electrical fields. This fact is due to the general opinion of quasi-ballistic transport in semiconductors. The possibility of quasi-ballistic transport in high resistive materials is counter intuitive and have therefore never been sought for so far. The understanding of the essential physics of this quasi-ballistic transport process have been that, as long as the applied electrical field E is within ohmic range (mobile charge carriers' concentrations and electrical mobility are constant and independent of the electric field E) and the thickness of the said piece of semiconducting or insulating material is larger than the mean free path of the mobile charge carriers (at best of the order of some one to two thousand Angstroms), then the current component from ballistic electrons is negligibly small, leading to essentially zero value of electron emission. (For references, see S.M. Sze: Physics of semiconductor devices; John Wiley 1981 or K.W. Boer: Survey of semiconductor physics, vol. II; Van Nostrand Reinhold 1992)

1. Electron transmitting Semiconductors

The quasi-ballistic transport of electrons in high resistivity semiconductors or insulators, when exposed to small (around 100 V/cm) electric fields, is a property, which can be used in more or less any semiconductor component or device.

Semiconductor components and devices cover a vast field of applications and the patents and references within the area are numerous. Four major classes of applications have been made with examples of products in each class.

- Class A: Rectification and charge (information) storage.
  Semiconductor components/devices in this class include Schottky barrier diodes (US5 627 479 and EP672 257 B1), bipolar p - n, p - i - n diodes, thyristors as well as a number of unipolar devices such as MIS (Metal - Insulator - Semiconductor) diodes, CCD (Charge - Coupled Devices), MIS tunnel diodes, MIS switch diodes, IMPATT (Impact Ionisation Avalanche Transit Time) and BARITT (Barrier Injection and Transit Time) diodes and other related Transit Time devices.

- Class B: Photo-Sensing and Photo-Emitting devices

This class of semiconducting components/devices include among others LEDs' (Light Emitting Diodes), Photodiodes, Semiconducting Lasers, Avalanche diodes and other photoconducting devices for light to electrical signal conversion purposes.

- Class C: Amplification and Non-volatile memory
  Applications of the present invention in this class of semiconductor components/devices include bipolar transistors and bipolar unijunction transistors, together with a number of unipolar components and devices inclusive FETs (Field Effect Transistor), JFETs (Junction Field Effect Transistor), MESFETs (Metal - Semiconductor Field Effect Transistor), MOSFETs (Metal - Oxide - Semiconductor Field Effect Transistor) and Non-Volatile Memory devices. Particularly relevant in relation to present invention within this class are tunnel transistors, TEDs (Transferred - Electron Devices) and other ballistic (Hot Electron) transistors and/or devices.
- Class D: Optical image detection, formation and processing
  Semiconductor camera, Conversion of electrical signals to 2D-optical images/signals, 2D-optical image/signal brightness/contrast amplification and spatial magnification.

Ballistic or hot electron devices as they are sometimes called, have been anticipated (see for example S.M. Sze: Physics of semiconductor devices; John Wiley 1981, p. 184, but also K.W. Boer: Survey of semiconductor physics, vol. II; Van Nostrand Reinhold 1992, p.1265 and 1247), but the proposed structures are costly to produce and unreliable, requiring extremely small dimensions (of the order of one hundred Angstroms) and high electrical fields.

2. Electron sources

The present invention relates to a general class of electron devices termed "electron sources" and more specifically to a subclass termed "planar electron sources". All of these devices provide a beam of electrons that can move through the empty space and be used for various technological applications.

The essential requirement for all electron sources is to provide sufficient amount of electrons at the emitting surface of the device (the surface of the device facing the vacuum) with sufficient amount of energy (3-5 eV in most cases) and a velocity in the direction of emitting surface in order that these electrons can surmount the energy barrier at the

emitting surface - vacuum interface and escape from the material into vacuum. The energy barrier is roughly given by the energy difference between the vacuum level and the electron chemical potential at the emitting surface. The necessary amount of energy can be supplied by any of the following means:

- Heating the emitting surface ("Thermal emission" electron sources)
- Establishing a sufficiently high electrical field in the region emitting surface-vacuum ("Field emission" electron sources).
- Sufficient acceleration of electrons within the bulk region of the device in the direction towards the emitting surface ("Tunnelling field emission" and/or "Quasi-ballistic field emission" electron sources).
- Illumination of the emitting surface with help of photons or other energetic particles ("Photo emission" electron sources).
- Lowering of the said energy barrier at the emitting surface-vacuum interface ("Negative electron affinity emission" electron sources).

or by the combination of any of the above methods.

While for some applications a point source electron beam is required, where the electrons are subsequently accelerated and electro-optically modulated, there are a large number of technological applications, where a planar source of electrons is required and/or would be advantageous. All of the prior art to be used in these applications, relate to small pointlike emission regions from a specific material detail at that point. A larger planar electron emitter can only be achieved by making an array of such small regions. Moreover, most devices need an opening in the anode for the electrons to escape into vacuum.

There is a very large number of inventions, as can be seen for example from citations in the US 5,703,435 (December 1997) and the US 5,534,859 (September 1996), that all relate to planar electron emitters with the main emphasis on the use of these inventions as basic building blocks in field emission Flat Panel Displays.
Most of the prior art can be broadly divided into two classes.

Class 1

In the first class the emitting cathode - anode structures are usually of all solid state construction and are formed from a combination of metallic, semiconducting and insulating

materials in order to establish the necessary conditions for the electron field emission to take place at the anode surface-empty space interface. The intentions of these devises are to improve electron emission efficiency, all using the same basic cathode with several substances disposed thereon. Electrons are emitted from the semiconductor surface into free space though an aperture of the anode. The principle is to narrow the semiconductor-free space barrier and to give the electrons the momentum to escape and/or tunnel through the electric potential barrier of an anode. Any of the above mentioned means can be applied in order to increase the electron emission current I_{em}.

It is a particularly characteristic feature of a majority of solid state devices in class one of the prior art, that the necessary large external voltages have to be applied over relatively very short distances (of the order of the electron mean free path), in order to generate sufficiently strong electric fields that facilitate the generation and the acceleration of electrons. These electrons then travel along what could be called quasi-ballistic trajectories in the said strong electric field (usually undergoing also an avalanche multiplication here) towards the surface of the emitting anode. At the same time however, they loose, on their way, an appreciable amount of energy through inelastic collisions (scattering). The present understanding is that large voltages are needed in order to obtain considerable emission of electrons through this method. If the applied electrical field E is to small (within ohmic range, mobile charge carriers' concentrations and electrical mobility are constant and independent of the electric field E) and the thickness of the semiconducting or insulating material L_{sam} (Figure 2) is larger than the mean free path of the mobile charge carriers (at best of the order of some one to two thousand Angstroms), then the electrical current component I_{bal} is negligibly small, leading to essentially zero value of the electron emission current I_{em} (Figure 2).

Some selected prior art of class 1 are commented below, others are referred in the end of the paragraph.

US 5,536,193 Relates to a method of fabricating a field emitter using the steps of; dispersing small pieces of wide band gap material on a substrate, cover it with a metal, etching the metal away until the wide band gap material comes forth, making small peaks for emitting electrons.

US 5,463,275 Describes only electron emitting devises comprising a layered structure of at least three specially chosen semiconductor materials

US 4,801,994 Relates to a three-layer semiconductor structure, where the middle layer is supposed to be an intrinsic semiconductor, which supposedly should conduct electrons with very low losses.

EP 504 603 B1 Consists of disposing a complex structure of semiconductors with special impurity levels such as to influence the different depletion regions. The description discloses the use of a Schottky barrier metal-semiconductor junction in order to improve emission efficiency.

US 5,554,859, US 4,303,930 and GB 1 303 659 cover areas similar to EP 504 603 B1

Other relevant references are: Metal-Insulator-Metal electron field emitters (Physical Review Letters Vol. 76, **17** (1996), 320), but also electron field emitters containing various forms of diamond-like components (US 5,631,196, US 5,703,435 and the citations there-off).

Class 2

In some cases of the said prior art, the features characterising class one (combination of more or less planar metallic, semiconducting and insulating materials of various thickness) are combined with feature concerning the formation/concentration and shaping of the necessary electrical field. The emitting cathode in this case is usually prepared in order to facilitate electron field emission from a single point. This is obtained either through covering the material with a low electron work function at small local areas and/or shaping the material geometrically to create an emissive point or peak.

Some selected prior art of class 2 are commented below, others are referred in the end of the paragraph.

US 5,229,682 Concerns a field electron emission device, in which electrons enter free space directly from a part of the emitting electrode pointing through an aperture in the opposite electrode and interjacent layer. The electrons are not traversing any interjacent semiconductor or insulator layer. The emitting electrode is shaped in order to have a part

that peaks through the aperture in the opposite electrode and interjacent layer. A flat panel display is made by an array of such electrodes.

US 5,712,490 Concerns a photocathode device, comprising several semiconductor layers disposed on a window layer, the semiconductor layers chosen; to optimise the ability to absorb photons, that is photoconductivity, to increase the diffusion length of those electrons. The invention does not disclose an optically transparent electrode to be disposed between the window layer and the first semiconductor layer (see 3rd column, line 11)

US 5,528,103 As US 5,229,682, but also comprising *focusing ridges*, for the purpose of generating an electrical field causing the electrons emitted from the gate electrodes in between them, to converge into a narrow band, *not* for absorbing electrons. Moreover these electrodes/ridges have to be conductive (though otherwise stated in col. 7, line 27) in order to serve their purpose.

US 5,212,426 As US 5,229,682, but also comprising an integral control for each electrode (pixel) using built in transistors for controlling the supply of electric charge to each emitting electrode

US 4,823,004 Relates to a device for analysing the ballistic trajectories of electrons through a material, as well as gaining information about the material bulk structure by analysing the ballistic trajectories.

US 5,444,328 Relates to a method for building up high voltage electron emitting semiconductor structures in a way which makes electrically breakdown less probable.

US 5,631,196 As US 5,229,682, but with the emitting electrode being flat, the parts peaking through the aperture in the opposite electrode and interjacent layer being replaced by impurity doped diamond parts as the electron emitting substance.

Other relevant references are: US 4,683,399, EP 150 885 B1, EP 601 637 A1, US 5,340,997 and the citations there off).

Exceptions

Exceptions from above classes include devices in which electrons are emitted into the empty space between a cathode and the anode by applying sufficient electrical voltage between them. The emitting cathode in this case is usually either covered by a material with a low electron work function and/or it is geometrically shaped in order to facilitate electron field emission. An example of such a device is:

US 5,703,435 Concerns a field emission cathode in which the material of the electron-emitting layer comprises either a mixture of graphite and diamond crystallites or amorphic diamond.

Applications

In order to utilise electron transmitting semiconductors and electron sources in applicable devices, several extensions have to be made to the basic components described in the prior art.

The emitted electrons might not have the sufficient energy to serve their purpose and have to be further accelerated. This will typically be carried out by having an "accelerating electrode" at some distance from the emitting surface at a high positive electrical potential thereby accelerating the emitted electrons to higher energies in the interjacent empty space.

For the electron - light conversion purposes, the appropriate "luminophor" materials can be incorporated within the anode structure, the said anode structure being either an integral part of the cathode - anode structure or part of the "accelerating electrode" separated from the cathode-anode structure by a finite empty space.

The applications of electron source devices typically include all forms of electron microscopy, Planar electron beams lithography, electron guns for evaporation of materials, x-ray tubes, electron multipliers (photomultipliers, two-dimensional particle/EM radiation detector arrays), electron beam welding machines, Flat Panel Displays (based on electron field emission), and some fast ballistic semiconductor components and devices.

Lithography prior art

A single very important application of the present invention is in the field of Lithography (Microlithography) and more specifically in the field of what has been termed in the literature as Planar Electron Beam Lithography (PEBL). Lithographic steps are essential during the process of Integrated Circuit (IC) production. The lithographic part of IC production consists in principle in repetition of the steps of resist deposition onto the surface of a wafer, of the exposing parts of the resist with radiation (photons, electrons or ions) by a "writing tool", and finally of resist removal. Optical, x-ray and Electron/Ion Beam Lithographs are the known methods that can, at least in principle, accomplish the necessary lithographic tasks during the IC production. The optical lithography is the standard, well-matured industrial technology; its major drawback is the optical diffraction limit on the smallest features that can be printed. In the further strife for decreasing the size of the IC components and ICs in general, this has to be considered as a major drawback. By using electrons as radiation source, the optical diffraction limit is not present. The schematic diagram of the principle behind the Planar Electron Beam Lithography, used in the prior art, is shown in Figure 8. It uses a basic structure consisting of cathode 1, a thin dielectric film 24, an electron absorbing template 19 and the anode 4. Electrons quantum tunnel through thin dielectric film 24 and emerge into free space FS through the surface S4 only at places, where the anode is in direct contact with the dielectric film. These electrons are then accelerated and projected onto the wafer with pre-deposited electron sensitive resist layer 6. In H. Ahmed et al (incl. some of the inventors of the present invention) "Proceedings of the Conference on Microlithography"; Cavendish Laboratory, Cambridge 1989, it is shown and demonstrated experimentally how to carry out Planar Electron Beam Lithography in practice. In this prior art, the electron lithographic projection system has been demonstrated using a prior art planar electron emitter. However, the accessible electron emitters suffer from other drawbacks: Planar electron emitters suitable for this purpose can expose entire wafers with one broad beam, but, at the necessary voltages, these planar electron emitters have extremely short lifetimes due to the effects caused by the necessary large fields and short distances.

The present invention offers a solution to this problem.

It is a disadvantage of the existing field emission planar electron devices, that large external voltages have to be applied over relatively very short distances (of the order of the

electron mean free path) in order to generate sufficiently strong electric fields that facilitate the generation and the acceleration of electrons.

It is another disadvantage that this requirement of relatively very high local electrical fields over relatively very short distances, together with the quality of the material at hand, lead in its consequence, to shorter electron mean free path (larger scattering rates) that in turn effectively sets the limit on possible physical distances within the said devices that electrons can move through without too appreciable energy losses.

It is a further disadvantage that, due to the above mentioned effects, either only a small portion of these electrons have sufficient energy to escape through the (emitting) surface of the anode into a space next to the cathode - anode structure.

It is a still further disadvantage that these devices in general have quite low electron emission currents I_{em} (Fig. 2) and high background current I_{back} (Fig. 2),

It is a still further disadvantage of the existing field emission planar electron devices, that they suffer from shortcomings such as too large electrical power consumption per square centimetre of electron emitting surface,

It is a still further disadvantage that the above mentioned effects results in low electron emission efficiency.

It is a still further disadvantage of the existing field emission planar electron devices that they are often unstable and liable to dielectric breakdown that generally seriously limits their lifetime.

It is a still further disadvantage of said devices that they suffer from frequently overheating due to large energy losses in the critical areas of the said devices (high electric fields over very short distances).

It is a still further disadvantage that scaling-up of these planar electron field emission devices (increasing the electron emitting area of the cathode) poses a severe problem.

It is a still further disadvantage of said devices that they use non-standard expensive materials.

It is a still further disadvantage of the existing field emission planar electron devices, that the constructions are too complex.

It is a still further disadvantage of the planar electron emitters emitting a broad beam suitable for the exposure of wafers in the fabrication of IC's, that they have an extremely short lifetime (less than 30 minutes), which makes them unsuitable for Planar Electron Beam Lithography.

Electron transmitting semiconductors

The present invention aims at solving the above mentioned disadvantages by using the existence, under proper operating conditions and in certain simple semiconductor and insulator structures, of quasi-ballistic electrons.

It is an object of the present invention to make available a semiconductor or insulator substrate in which electrons move along quasi-ballistic trajectories when said substrate is subjected to low applied external electric fields ($\leq$100 V/cm). The electrons (quasi-ballistic electrons) move along these trajectories from one side of the substrate (surface S2, Figure 3) to the other side (surface S4), and are accelerated to energies sufficient to escape into vacuum through the electron emitting surface S4. (From now on said substrate is also referred to as Quasi-ballistic semiconductor substrate - "QB-Sem substrate").

It is another object of the present invention to make available a QB-Sem substrate in which the quasi-ballistic electrons suffer almost no energy losses and momentum changes while moving through the QB-Sem substrate.

It is a further object of the present invention to make available a QB-Sem substrate in which no heat is generated when the substrate is used for quasi-ballistic transport of quasi-ballistic electrons.

It is a still further object of the present invention to make available a QB-Sem substrate in which quasi-ballistic transport is possible at low (ohmic) electrical fields and can take place over macroscopic distances.

It is a still further object of the present invention to make available a QB-Sem substrate in which electron velocities are not limited by high electrical field mobility saturation effects.

It is a still further object of the present invention to make available a QB-Sem substrate in which the electron behaviour is similar to the behaviour of electrons in vacuum tubes.

It is a still further object of the present invention to make available a QB-Sem substrate, which do not require high electrical fields and extremely small substrate thickness (of the order of one hundred Angstroms).

It is a still further object of the present invention to make available a QB-Sem substrate from which simple design, robust, relatively cheap, high reliability and long lifetime semiconductor components can be produced.

It is a still further object of the present invention to make available a QB-Sem substrate to be used in the field of electron-optical applications.

It is a still further object of the present invention to make available a QB-Sem substrate to be used in the design and production of semiconductor components and devices and Integrated Circuits (ICs).

It is a still further object of the present invention to make available a QB-Sem substrate in which the anomalously low power dissipation by QB-electrons within the QB-semiconductor contributes to the solution of the heat generation problem when high packing densities of components in the ICs are used.

It is a still further object of the present invention to make available a QB-Sem substrate so that the design of "Hot Electron" devices does not have to rely on thin film complicated multistructures that are often unreliable and costly to produce.

It is a still further object of the present invention to make available a QB-Sem substrate, which do not require high electrical fields, so that the degradation of the various semiconductor devices through irreversible dielectric breakdown is essentially eliminated.

It is a still further object of the present invention to provide QB-Sem substrates, which are fully integrable with the existing Semiconductor Technology.

It is a still further object of the present invention to provide QB-Sem substrates, which are fully integrable with the existing Integrated Circuit Technology and Production.

It is a still further object of the present invention to provide QB-Sem substrates from which the design of fast high frequency semiconductor components and devices are under no geometrical constraints.

It is a still further object of the present invention to provide QB-Sem substrates with which new design concepts for semiconductor components/devices and/or physical apparatuses are possible.

It is a still further object of the present invention to provide QB-Sem substrates with life times of the same order of magnitude (or longer than) as the usual Semiconductor Industry products.

The effect that, in QB-semiconductors, electrons that can move quasi-ballistically over macroscopic distances at low applied electrical fields, as disclosed by the present invention, will have a major impact on design and construction/manufacture of many semiconductor components and devices of both bipolar and unipolar variety. These will be used either as single units or as components/parts within Integrated Circuits' architecture.

Electron sources

It is an object of the present invention to provide electron emitters in which the emitted electrons use macroscopic quasi-ballistic trajectories (these trajectories are many hundreds of microns long) in a piece of QB-Sem substrate subject to low externally applied electrical fields ($\leq$100 V/cm). These electrons (quasi-ballistic electrons), moving along these trajectories from one side of the substrate (surface S2, Figure 3) to the other (surface

S4) are accelerated, increasing thereby their energy, and escape into vacuum through the electron emitting surface S4.

It is another object of the present invention to provide planar electron emitters, which are characterised by very low applied electric fields/voltages.

It is a further object of the present invention to provide planar electron emitters, which are characterised by very low power dissipation.

It is a still further object of the present invention to provide thin (≤1 cm) planar electron emitters with all solid state construction.

It is a still further object of the present invention to provide planar electron emitters in which the macroscopic emitting surface has no subdivisions.

It is a still further object of the present invention to provide planar electron emitters characterised by the simplicity and robustness of the assembly (Figure 3).

It is a still further object of the present invention to provide planar electron emitters characterised by the self supporting structure of the assembly.

It is a still further object of the present invention to provide planar electron emitters in which there are no limits to geometrical scaling-up of electron emitting surface.

It is a still further object of the present invention to provide planar electron emitters in which the electron emission area is large and only limited by the lateral size of the QB-semiconductor wafer, which is today some 800 cm2 (this limit can be of course be overcome by building modules).

It is a still further object of the present invention to provide electron emitters suitable for Planar Electron Beam Lithography

The number of technological applications of the planar quasi-ballistic electron emitter is very large and it is the intention of the authors of the present invention to claim also the use of the present invention in these. These applications include methods and

apparatuses/products such as Planar electron beam lithography, Field emission Flat Panel Displays, High speed (low-dissipation) signal transmission devices, High efficiency detectors, efficient Light sources, Electron emission microscopy, Two-dimensional electromagnetic radiation and/or particle detector arrays, High speed, easily integrable semiconductor components, Semiconducting devices using ballistic electrons, variety of (novel) electron sources and many others.

SUMMARY OF THE INVENTION

The above mentioned objects are complied with by providing, in a first aspect, an article comprising

- an element having a first and a second surface, wherein

  - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, the first surface being substantially parallel to the second surface, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- means for providing an electric field across at least part of the element, said means comprising

  - means for providing the first electrical charge to the first surface of the element, and

  - means for providing the second electrical charge to the second surface of the element, the second electrical charge being different from the first electrical charge in order to move electrons in a direction substantially perpendicular to the first or the second surface.

In a second aspect, the present invention relates to an article comprising

- an element having a first and a second surface area, wherein

  - the first surface area is adapted to hold a first electrical charge, and wherein the second surface area is adapted to hold a second electrical charge, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- means for providing an electric field across at least part of the element, said means comprising

  - means for providing the first electrical charge to the first surface area of the element, and

  - means for providing the second electrical charge to the second surface area of the element, the second electrical charge being different from the first electrical charge in order to move electrons between the first surface area and the second surface area.

The material or material system according to the first and second aspects may comprise a semiconductor, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

In order to reduce electron scattering, and thereby facilitate the presence of quasi-ballistic electrons, the material or material system may be doped with one or more of the following dopants: phosphorus, lithium, antimony, arsenic, boron, aluminium,

tantalum, gallium, indium, bismuth, silicon, germanium, sulphur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium. The predetermined doping level may be less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

The means for providing the first electrical charge to the first surface may comprise an at least partly conductive first material or material system. In a similar way, the means for providing the second electrical charge to the second surface may comprise an at least partly conductive second material or material system.

The at least partly conductive first and second material or material system may constitute thin layers each having a first and a second surface. The layers may comprise one or more of the following materials: gold, chromium, platinum, aluminium, copper, caesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

In order to provide energy to the system the second surface of the first layer may be operationally connected to a first terminal of a charge reservoir, whereas the first surface may be in direct contact with the first surface of the material or material system of the element. Similarly, the first surface of the second layer may be operationally connected to a second terminal of the charge reservoir, whereas the second surface is in direct contact with the second surface of the material or material system of the element.

The charge reservoir may comprise a battery or any other electrical energy source capable of providing a direct or alternating current to the article.

The first and second layer may comprise a metal or a highly doped semiconductor material with a doping level higher than $1x10^{17}$ cm^{-3}.

In a third aspect, the present invention relates to a method for providing a first type of electrons, said method comprising the steps of:

- providing an element having a first and a second surface, wherein

- the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, the first surface being substantially parallel to the second surface, and wherein

- the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- providing means for providing the first electrical charge to the first surface of the element, and

- providing means for providing the second electrical charge to the second surface of the element, the second electrical charge being different from the first electrical charge so as to move a second type of electrons in a direction substantially perpendicular to the first or second surface.

In the present context, the first type of electrons may comprise electrons traversing the element with normal losses, whereas the second type of electrons may comprise quasi-ballistic electrons.

The material or material system forming at least part of the element may comprise semiconductor materials. A list of suitable materials or combinations thereof have been mentioned in relation to the first and second aspects of the present invention. Similarly, the preparation may comprise doping using the above-mentioned dopants and doping levels in order to reduce scattering of quasi-ballistic electrons.

In order to move quasi-ballistic electrons a potential difference larger than 2 volts may be applied between the first and second surface of the element. Suitable materials or material systems for providing the first and second charges to the element may comprise a metal or a highly doped semiconductor material with a doping level higher than $1x10^{17}$ cm^{-3}. Examples of such materials are: gold, chromium, platinum, aluminium, copper, caesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

In a fourth aspect, the present invention relates to a method for fabricating an article, said method comprising the steps of:

- providing a semiconductor material or material system having a first and a second surface, the second surface being substantially parallel to the first surface, the semiconductor material or material system having a predetermined crystal orientation perpendicular to the first or second surface,

- providing a surface treatment to the first and second surfaces so as to reduce surface roughness,

- doping the semiconductor material or material system with a dopant so as to obtain a predetermined doping level so as to reduce electron scattering within the material or material system,

- providing an at least partly conductive first material or material system, said first material or material system forming a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element, and

- providing an at least partly conductive second material or material system, said second material or material system forming a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

Regarding the above-mentioned materials or material systems a list of suitable candidates or combinations thereof have been mentioned in relation to the first and second aspects of the present invention. Similarly, the preparation may comprise doping using the above-mentioned dopants and doping levels in order to reduce scattering of quasi-ballistic electrons.

The predetermined crystal orientation may comprise the <111>, <110> or <100> direction, or any other crystal orientation appropriate for the crystal structure of the element. The surface treatment may comprise different kinds of techniques such as etching and/or polishing. Polishing may comprise optical and/or mechanical polishing.

Regarding dopants, these may be selected from the group consisting of lithium, phosphor, antimony, arsenic, boron, aluminium, tantalum, gallium or indium or any combination thereof. The doping level may be less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

The at least partly conductive first and second material or material system may comprise a metal or a highly doped semiconductor material with a doping level larger than $1x10^{17}$ cm^{-3}. Suitably materials may comprise gold, platinum, chromium, aluminium or copper or any combination thereof.

In a fifth aspect the present invention relates to a flat panel display comprising

- an article according to the first aspect of the present invention, the article further comprising

  - a layer of material being adapted to emit light at a plurality of wavelengths upon exposure of electrons, said material layer defining, in a plane substantially parallel to the first and second surface of the element, a two-dimensional matrix having one or more surface elements, each surface element being adapted to emit light at a predetermined wavelength, and

  - means for selectively proving electrons to the one or more surface elements in the two-dimensional matrix.

The material layer for emitting the plurality of wavelengths may comprise an appropriate luminophors or standard colour television phosphors. The material layer

may be held by the first or second surface of the element. Alternatively, the material layer may be held by an additional element.

In order to obtain full colour information the emitted light may comprise at least three wavelengths corresponding to at least three colours. By combining these three colours it should be possible to deduce any colour in the visible range. The emitted wavelengths may correspond to colours red, yellow and blue, or to colours red, green and blue.

The selective means may comprise a pattern so as to define, in a plane substantially parallel to the first or second surface, a two-dimensional matrix of electrically controllable matrix elements, said pattern being formed by the at least partly conductive material or material system.

In a sixth aspect, the present invention relates to a method for exposing a film, such as a resist, to a plurality of electrons of a first type, said method comprising the steps of:

- providing a first element having a first and a second surface, wherein

    - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, and wherein

    - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- providing a second element, said second element being adapted to hold the film to be exposed to the plurality of electrons of the first type,

- providing a patterned absorption layer, said absorption layer being adapted to absorb electrons transmitted through the first element at positions determined by the pattern,

- providing the first electrical charge to the first surface of the first element, and

- providing the second electrical charge to the second surface of the first element, the second electrical charge being of opposite sign compared to the first electrical charge so as to move a second type of electrons from the first surface towards the second surface, and

- providing a third electrical charge to the second element, said third electrical charge having the same sign as the second electrical charge.

Regarding the above-mentioned materials or material systems a list of suitable candidates or combinations thereof have been mentioned in relation to the first and second aspects of the present invention. Similarly, the preparation may comprise doping using the above-mentioned dopants and doping levels in order to reduce scattering of quasi-ballistic electrons.

The first and second electrical charges are provided to the first and second surfaces of the first element from a first and second terminal of a charge reservoir, respectively, wherein the potential difference between the first and second terminals of the charge reservoir is larger than 2 volts. The third electrical charge is provided to the second element from a third terminal of the charge reservoir.

The second element may comprise a metal or a semiconductor material, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

Finally the first type of electrons may comprise electrons traversing the element with normal losses, whereas the second type of electrons may comprise quasi-ballistic electrons.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic and simplified electron energy band diagram according to present invention, when the applied external potential is zero.

Figure 2 is schematic and simplified electron energy band diagram according to present invention, when a finite external potential is applied.

Figure 3 is a simplified model of the basic structure of a planar electron emitter according to the present invention.

Figure 4 is a schematic side view if a flat panel display showing the patterned electrodes and luminophor, the latter being placed between the QB-Semiconductor substrate and the anode.

Figure 5 is a top view of Figure 4.

Figure 6 is an alternative embodiment to the flat panel display according to Figure 4, in which the luminophors are placed after the anode.

Figure 7 is another alternative to the flat panel display according to Figure 4, in which an electron acceleration electrode are incorporated, and the luminophors are placed after the accelerating electrode.

Figure 8 is a schematic side view of a prior art planar electron emitter for Planar Electron Beam Lithography. A template of electron absorbing material is placed between the QB-Semiconductor and the anode. An electron acceleration electrode is added, and the substrate to be exposed is placed before this electron acceleration electrode.

Figure 9 is an alternative embodiment according to Figure 8, in which the substrate to be exposed is placed after the electron acceleration electrode and outside the vacuum while the total structure of QB-Semiconductor and electrodes are placed in vacuum.

Figure 10 is equivalent to Figure 8 but with a planar quasi-ballistic electron emitter according to a preferred embodiment of the present invention.

Figure 11 is a schematic drawing of an apparatus for implementing planar quasi-ballistic electron emitters in Planar Electron Beam Lithography.

Figure 12 is a photograph of the apparatus of Figure 11.

Figure 13 is one possible template as mentioned under Figure 10.

Figure 14 is a scanning electron microscope photograph showing some structures made by Planar Electron Beam Lithography.

Figure 15 is a 3D view showing the interior of the embodiment according to two-dimensional illuminating panels.

Figure 16 is a 3D view showing the exterior of the embodiment of Figure 15.

Figure 17 is an alternative embodiment according to two-dimensional illuminating panels.

Figure 18 is a schematic diagram of a typical, fast, planar Schottky barrier diode according to the present invention.

Figure 19 is schematic and simplified electron energy band diagram according to the embodiments of Photo-Sensing and Photo-Emitting devices.

Figure 20 is a schematic diagram of a typical planar Metal - Semiconductor Field Effect Transistor (MESFET).

Figure 21 is a schematic diagram of a device according to the present invention for the detection and recording of two-dimensional optical signals/images.

Figure 22 is a schematic drawing according to the embodiment of an optical signal/image-processing device.

Figure 23 is a schematic energy diagram of one of the possible constructions of a solar cell according to the present invention.

Figure 24 is a schematic drawing according to the embodiment of an Electron Cold Emission Microscopy (ECEM).

DETAILED DESCRIPTION OF THE DRAWINGS

Description of the present invention, theoretical

The present invention will first be described theoretically using the embodiment of a Planar Electron Emitter (PEE) with reference to Figure 1 and Figure 2. Also, for the sake of clarity, without loosing the validity and generality of the arguments to follow, a simplified model will be used that also uses a specific set of electrodes. Under no circumstances this should be construed as limiting factor of the present invention The specific configuration in Figure 1 and Figure 2 is used purely for illustration purposes and other much more general and/or different configurations are possible and must be considered as covered by the present invention.

In Figure 1, a simple electron band structure as a function of spatial co-ordinate of a piece of semiconductor or insulator material is shown, where two, for the electrical transport most relevant, quantum mechanical energies E_v (top of the valence band) and E_c (bottom of the conduction band) are marked. The two energies E_c and E_v are separated by a band gap E_g. A set of two metal electrodes, 1 (cathode) and 4 (anode) are deposited on the two respective surfaces S2 and S3 of the said piece of semiconductor or insulator material. For the sake of simplicity these two electrodes are assumed to be identical.

At zero degrees Kelvin all quantum mechanical electron states above E_c and above chemical potential (μ_M^{ch}) of the metal electrodes are empty, while those below E_v and below chemical potential (μ_M^{ch}) of the metal electrodes are occupied. At some finite temperature, e.g. 300 degree Kelvin and in thermodynamical equilibrium, the chemical potential within the bulk of the said piece of semiconducting or insulating material (μ_B^{ch}) is assumed to lie somewhere near the middle of the gap. For the sake of simplicity it is assumed that this chemical potential coincides (in energy) with the chemical potential of the metal electrodes, forming in this way what is known as a neutral electrical contact. At this finite temperature there will be a small but finite concentration n_e of mobile electrons at energy E_c and small but finite concentration n_h of mobile holes at E_v. It is assumed furthermore that the semi-

classical approximation is valid which means that there are no changes in the electron band structure locally when external electrical field E is applied. The effect of this field is accounted for by appropriate spatially dependent energy shift of all quantum mechanical energies at a given distance x due to the presence of the classical electrical potential

$$V(x) = E \cdot x . \qquad (1)$$

Figure 1 then describes in its totality the situation at finite temperature when no external electrical field is applied.

The situation described in Figure 1 will change to situation described in Figure 2, when a finite, negative electrical charge ΔQ is added to metal electrode 1 and corresponding negative electrical charge ΔQ is removed from metal electrode 2. These extra charges on the two said electrodes will cause a constant electrical field E to be present within the said piece of semiconducting or insulating material.

Under low, ohmic electrical field E (~ 100 V/cm; see also Figure 2), the mobility and the concentrations of thermal electrons n_e and holes n_h (Figure 2) will stay essentially constant, while their drift velocities will change accordingly

$$\text{V-drift (electrons; holes)} = \text{mobility (electrons; holes)} \cdot E , \qquad (2)$$

increasing in this way the respective currents I_e and I_h (Figure 2) with increasing applied electrical filed E. The component I_{bal} (Figure 2) is the contribution to the total electrical current running through the structure shown in Figure 2 from quasi-ballistic electrons, that is those electrons, injected into said piece of semiconducting or insulating material from the metal electrode 1, that essentially do not suffer any inelastic energy losses nor any appreciable momentum changes while moving through the said piece of semiconducting or insulating material towards the metal electrode 2 along the electron quasi-ballistic trajectory shown in Figure 2. The electrical current component I_{em} is due to those electrons (quasi-ballistic electrons) which, after traversing from the metal electrode 1, through the said piece of semiconducting or insulating material and into the metal electrode 2, have still sufficient energy (energy larger than the energy barrier of the emitting surface S4 - Free Space interface) and finite, sufficiently large velocity component in x- direction in order to escape from the structure, composed of the metal electrode 1 plus the said piece of

semiconducting or insulating material plus metal electrode 2, into free space (FS in Figure 2) through electron emitting surface S4 (Figure 2).

QB-Sem

The preparation of the individual regions of the quasi-ballistic electron transmitter/emitter are now described

In reference to Figure 3 now the preparation of a high resistive semiconductor or insulator will be described. The quasi-ballistic semiconductor (QB-Sem) in this case was the said single crystal silicon sample, cut out from a single crystal Si ingot, prepared by a Float Zone crystal growth method. Thin slices (wafers) were prepared from this ingot, with <111> orientation perpendicular to the wafer surface. However, other lattice orientations <110> and <100> can also be chosen with similar results. If a material crystal other than Silicon is used, lattice orientations appropriate for such material crystal should be chosen. Both surfaces S2 and S3 were optically polished. The Phosphorus doping level (giving n-type conductivity) was chosen to be $2.0 \cdot 10^{12}$ cm -3. A Schottky contact (a cathode) was prepared by a successive evaporation of 50 Å of Chromium onto the surface S2 followed by evaporation of 2000 Å of Gold. The anode was ohmic, consisting of high Phosphor concentration, degenerate silicon layer (a thin region appr. ~1 microns thick, below the surface S3 - see Figure 3) and a thin 150 Å thick evaporated Gold film.

The region 2 - Quasi-ballistic semiconductor

The choice of the quasi-ballistic semiconductor is not limited to one particular material, but can be prepared in a number of different ways, using different materials. The only requirements are the existence of a finite band gap E_g (see Figure 1) and the existence of quasi-ballistic trajectories for electrons between the two opposite surfaces of the material. In the preferred embodiment the said material (QB-Sem) is silicon, but group III - V compound semiconductors (such as GaAs) and group II - VI compound semiconductors are also equally good candidates. Crystallographic orientation, shallow and deep impurities doping levels and the temperature of operation of the finished device are the important parameters to consider when choosing a suitable quasi-ballistic semiconductor.

Also well suited as Quasi-ballistic semiconductor (at least in principle) are insulators such as SiO_2, Al_2O_3, Silicon carbide, silicon nitride, diamond (or diamond-like Carbon particles) and others. Some of the materials have been and/or are being investigated in connection with their use as field emission electron sources already (see prior art).

Region 1 and surfaces S1 and S2 - Cathode region

In the preferred embodiment depicted in Figure 3, the cathode region has been formed by evaporation of Chromium and Gold metal films onto the surface S2 of the silicon sample, forming in this way a rectifying Schottky contact. The sole purpose of the cathode region though is to maintain various amount of negative charge ΔQ on the surface S2 and this can be done in a number of different ways.

In one such alternative, the region 1 is just a gaseous phase of partially ionised gas such as Argon and/or Nitrogen. No metal electrode is required in this case at all.

To achieve the optimal performance of the cathode as an electron injector of electrons into the QB-semiconductor region (2 in Figure 3), it is desired that the said extra negative charge ΔQ from the battery (see Figure 3) moves the chemical potential μ_M^{ch} (see Figure 2) as much as possible (increase of the electron injection into QB-Sem). This can be achieved by decreasing the interface electron density of states through mechanical, chemical and/or thermal treatment of the surface S2. If the metal cathode electrode is either required or desired, this treatment of the surface S2 is done prior metal material deposition. Alternatively, one can choose a metallic material with low electron density of states at the Fermi level and/or low electron work function.

Region 4 and surfaces S3 and S4 - Anode region

As described above, a thin region of silicon sample, next to the surface S3, has been implanted with high dose of Phosphorus, becoming in this way degenerate. A thin Gold film has been then deposited on the said surface S3 which has been optically polished prior this Gold film deposition, the whole structure forming in this way an ohmic contact to the silicon sample. This preparation of the anode region might not lead to the most optimal performance of the said Planar Electron Emitter PEE.

As with the cathode region, the sole purpose of the anode region is to secure that a various amount of negative charge ΔQ can be removed from the surface S3 region. Here though, the requirements concerning the optimal functioning of the said (anode) region are different from those valid for the cathode region. The hole current I_h (see Figure 2) should be minimised (current I_h increases as the interface chemical potential μ_M^{ch} moves downwards in energy - see Figure 2) as well as the thickness of the anode metal electrode (relatively large energy losses of the quasi-ballistic electrons when moving through region 4). To achieve the first of these goals one needs either a metal with very high electron density of states at the Fermi level and/or very high electron density of states within the surface S3 - region 4 interface. As with the preparation of the surface S2, also here this can be achieved with the proper mechanical, chemical and/or thermal treatment of the said surface S3 prior metal deposition.

In order to achieve the second goal, yet another alternative can be chosen. In this case the surface S3 is free of the metal electrode (region 4 in Figure 3) and an extra electrode (electron acceleration electrode 7 - see Figure 8 for example) is placed within the free space FS (Figure 3) and in closed vicinity of the surface S3. This extra electrode is biased at relatively high positive potential with the respect to surface S3 and/or the cathode region 1, polarising in this way the whole assembly. If the developed electric field within the region 2 is not sufficient for the acceleration of the quasi-ballistic electrons within the region 2 to energies required in order for these electrons to escape through the said surface S3 into free space FS, the surface S3 can be geometrically shaped in such a way as to increase the said electric field locally at points (and/or sharply curved regions) of the surface S3, spatially closest to the electron acceleration electrode 7 in Figure 8.

Finally, the geometrically shaped surface S3 can be covered by a thin metal electrode (serving as a anode), the whole Planar Electron Emitter assembly (inclusive the electron acceleration electrode 7) looking similar to an arrangement shown in Figure 8. In such an arrangement the electrical discharging/charging up effects on the geometrically shaped surface S3 are minimised.

The important point to stress here is that the shape of the electron emitting surface S3 (surface S4 if metal electrode 4 is present) does not have to be strictly planar.

Performances of QB-Sem

The sample was placed in the vacuum and at external voltage of some 4.0 Volts (forward bias) between the cathode and the anode (at four volts across 0.5 millimetre - the thickness of silicon sample, the electric filed of 80.0 Volts/cm was created within the bulk of the silicon sample) a finite, relatively large and laterally homogeneous electron emission current I_{em} was observed. The magnitude of the emission current I_{em} indicated that as much as some 30 % of all electrons, injected into the silicon sample from the cathode, reached the anode with energies of some 4 eV (electron affinity in silicon is 4.0 eV) above the energy E_c (see Figure 2), sufficient in order for these electrons to surmount the energy barrier of the anode surface S4 - vacuum interface and to escape into the free space FS (see Figure 3).

Description of the present invention, practical

The present invention will first be described practically using the embodiment of a Planar Electron Emitter (PEE) with reference to Figure 3 which is a schematic diagram illustrating one of possible physical forms of the preferred embodiment according to present invention.

The region 1 (a cathode) is connected both to region 2 (a piece of quasi-ballistic semiconductor) via surface S2 and to a negative pole of an external electrical charge/voltage supply 8 (battery) via electrical contact pads (ECP). Its role (cathode), together with the battery, is to supply and to maintain the negative electrical charge ΔQ (electrons) on the surface S2. At the same time, the same negative electrical charge ΔQ is removed from the region 4 (anode). The anode is connected to region 2 via surface S3 and to a positive pole of the external charge/voltage power supply 8 via ECP, the said power supply 8 maintaining the surface S3 positively charged. In this way a uniform electrical field E is established between the surfaces S2 and S3, causing a finite electrical current I_{tot} to flow through the region 2. In reference to Figure 2 now, this electrical current I_{tot} is composed of three components I_e, I_h and I_{em}. While the first two components form the background electrical current I_{back}, the component I_{em} is formed by that portion of the electrons (from now on termed as quasi-ballistic electrons) that physically leave the device and enter the free space FS (Figure 3) if a sufficiently high electrical field E and the corresponding electrical potential difference (V = E. t1 is maintained between the surfaces S2 and S3.

When a piece of semiconducting or insulating material (region 2 - from now on termed as QB-Sem) is properly prepared, the surfaces S2 and S3 are properly treated and the regions 1 and 2 are properly chosen and constructed, the part of the electrical current I_{em} (electron emission current) can become quite large in relation to the background current I_{back}.

When QB semiconductor is properly chosen and prepared, then even without any efforts for optimisation (inclusive the optimisation of the surfaces S2 and S3), I_{em} of hundreds of nano-Amperes per square centimetre can be measured at electrical fields of the order of some 100 Volts/cm (from now on termed as ohmic electric fields), with the total thickness of the device L2 being macroscopic (less than millimetres). With the length scale L1 (square root of the area of the device) being of the order of 30 cm (today's size of silicon wafers for example), the device depicted in Figure 3 is a large area planar electron emitter that is very simple to manufacture and can be produced at a very competitive price, even when compared with the standard Cathode Ray Tube (CRT) TV screens.

In the preferred embodiment depicted in Figure 3, a sufficient injection of electrons from the cathode into the silicon sample ("Injection of electrical charge" - see Figure 2) has been achieved electrically, by supplying the metal electrode 1 (cathode) with extra amount of negative charge ΔQ from the battery. However, since the electron injection from the cathode region into QB-semiconductor is also strongly temperature dependent, an alternative embodiment of the Planar Electron Emitter according to the present invention can involve a heated cathode structure (region 1 - see Figure 3). In yet another alternative embodiment, the electrons are injected into the QB-semiconductor by photo-illumination of the cathode-injecting surface S2 region (in some cases this region can include part of the QB-semiconductor next to the surface S2) through the surface S1. This embodiment of the said Planar Electron Emitter PEE according to the present invention is particularly useful in opto-electronic applications. These methods for electron injection will be described in the descriptions of the relevant preferred embodiments in the following sections.

The Planar Electron Emitter (PEE) according to the present invention has now been demonstrated through a description of one preferred embodiment shown in Figure 3. There exists however a large number of other embodiments, all according to the present invention, that relate to different choice of materials, of design and of preparation and

construction of the said Planar Electron Emitter, the said differences being dictated by the requirements of the applications at hand. It should be stressed that even though electrons are emitted into free space in the PEE used to describe the basic principles of QB-semiconductors, it is not a demand. As some of the other possible embodiments will show, the basic characteristic of QB-semiconductors, the quasi-ballistic transport of electrons, can also improve many non-emitting semiconductor devices.

Examples of Applications (Description of the preferred embodiments)

A number of applications of the present invention, besides the planar electron emitter, will now be illustrated and discussed in some detail with reference to Figures 3 to 24. The generality of each application field using the present invention has to be stressed at this time, although each application field and/or product will be illustrated with a help of a specific preferred embodiment and relevant Figure(s). To each such preferred embodiment there exists a large number of other embodiments and/or modifications of the preferred embodiment, that all use the present invention as a crucial component. Therefore it is essential that the description of the present invention already given in the previous sections and the description of the applications of the present invention to be given in the following, are not construed as limiting the scope of the present invention and its applications.

Example 1. Field Emission Flat Panel Displays (FE-FPD)

One of the obvious applications of the present invention is its use in the construction of robust, reliable, large, low power dissipation and cheap Field Emission Flat Panel Displays (FE-FPD).

Figure 4, which is a cross-sectional diagram along the line A - A of the FE-FPD shown in Figure 5 is one of the possible vacuum-less FE-FPDs according to the present invention With reference to Figure 3, the basic planar structure of the present invention - 1(cathode), 2(QB-Sem) and 4(anode - optically transparent in this preferred embodiment) is clearly apparent also in Figure 4. The only difference is that in this Flat Panel Display application of the present invention the cathode and the anode are patterned and that an extra layer 3 is introduced between the surface S3 of the QB-semiconductor and the anode 4. This third layer consists of alternative (patterned) segments of red 5, yellow 18 and blue 11

phosphors or other colour light emitting luminophor. The segments are separated from each other by light non-emitting, electron absorbing material 16.

The patterning of layers 1, 3 and 4 enables selective addressing ("switching-on" an element 23 (i, j) by application of the appropriate voltages) of the individual colour segments ("pixels") and is shown in Figure 5. Here the cathode 1 (in form of metallic parallel strips) is deposited onto the back surface S2 of the QB-semiconductor 2. Red 5, Yellow 18 and Blue 11 luminophor strips are deposited on the front surface S3 of the QB-semiconductor 2, in alignment with the said cathode strips, as shown in Figure 5. Finally the anode 4, also in form of metallic, parallel strips, is deposited on the top of the layer 3, with anode metallic strips at right angles to the cathode metallic strips, as indicated in Figure 5.

The electrical leads 9 and 10 are attached to the respective metallic strips of the anode and the cathode via electrical contact pads ECP, the whole cathode - anode structure forming in this way selectively addressable matrix of single colour light emitting elements. The element (i, j) is switched on by applying an appropriate voltage between the line i - (cathode) and the line j - (anode). The electrical leads 9 and 10 are connected to the usual TV a/c circuitry that drives the whole FE-FPD shown schematically in Figures 3, 4, 5, 6 and 7. The dimensions d1, d2, d3 and d4 of the pixel matrix can be optimised at will, using the standard semiconducting patterning technology to fit the spatial resolution requirements of FE-FPD at hand.

The typical over-all size L1 L2 of a "single chip" FE-FPD depicted in Figures 4, 5, 6 and 7 is at present of the order of 20 cm by 20 cm, with the availability of 30.0 cm diameter Si wafers. When large colour displays are needed, a arbitrary number of "single chip" modules can be joined together on an appropriate substrate, using the segments d2 and d4 (see Figure 5) as joining regions, preventing in this way the spatial degradation of the formed optical image quality. The thickness L3 of the said FE-FPD depicted in Figures 4, 5, 6 and 7 is of the order of one millimetre, this thickness being essentially the thickness of the QB-semiconductor wafer.

In Figure 6, the layers 3 and 4 are switched over in order to illustrate yet another possible physical form of the said FE-FPD. Here the colour light layer 3 faces directly the free space FS. If needed, the surface S5 can contain a protective, transparent (anti-reflection) coating.

It has to be stressed at this point that the segments 5, 6 and 11 shown in Figures 4, 5, 6 and 7 do not have to be necessarily luminophor. The colour light-emitting layer 3 represents also other types of electron-to-colour-light conversion materials and/or devices. One such type is an arrangement, which can be described with the help of Figure 4. In this case the structure 1(cathode), 2(QB-semiconductor), Red/Yellow/Blue) elements (5, 18, 11) and 4(anode) form a matrix of Colour Light Emitting Diodes (CLED). Other FE-FPD arrangements, using the present invention are of course also possible and the preferred embodiment shown in Figures 5, 6 and 7 should in no way considered as a limiting the scope of the present invention in this field of application.

Finally, in cases where the requirement of colour definition, brightness and colour contrast are not met with luminophors and/or other electron - light conversion elements/devices that are at hand today, the standard TV colour phosphors may be still needed that require quite high electron energies (high acceleration voltages in the region of some 10 to 20 kV). A vacuum Field-Emission Flat Panel Display may be then still a most optimal solution and one possible physical form, using the present invention, is shown in Figure 7.

In this configuration, the colour light emitting layer 3 shown in Figures 4, 5 and 6 is removed from the basic planar electron emitter structure 1(cathode), 2(QB-semiconductor) and 4(anode) and it is deposited on the optically transparent (glass for example) plate 13 that forms, together with parts 14 and 12, the vacuum encapsulation of the said vacuum FE-FPD. The electron acceleration electrode 7 that is deposited onto the layer 3 is biased to the appropriate high positive voltage. This arrangement secures that the quasi-ballistic electrons that leave the basic planar electron emitter structure (attached mechanically to the base plate 12 via mechanical supports 15) through the surface S4, are accelerated within the free space FS (now vacuum) to sufficiently high energies in order to secure the proper functioning of the standard colour TV phosphors 5, 6 and 11.

The thickness (Dim 2) of the vacuum FE-FPD shown in Figure 7 is of the order of one to two centimetres, while the area (Dim 1) is unchanged in relation to the previously described vacuum-less FE-FPD.

Example 2. Planar Electron Beam Lithography

By using the planar electron emitter according to the present invention the major drawback imposed by the short lifetime of the prior art planar electron emitters, are solved. The present invention offers a qualitatively new and robust solution to the present day needs of the semiconductor industry. The method and the embodiment are described in Figures 9 to 14.

The schematic diagram of the principle behind the Planar Electron Beam Lithography, was described in the prior art using Figure 8. In the prior art, an electron lithographic projection system has been demonstrated using a prior art planar electron emitter. The planar electron emitter of the present invention can be directly implemented in place of the prior art emitter.

One possible embodiment according to the present invention of such a planar electron emitter structure is shown in Figure 10. The major difference from prior art Figure 8 is the replacement of a thin film oxide layer 24 in Figure 8 by a quasi-ballistic semiconductor QB-Sem 2 in Figure 10. Turning now to Figure 10, the electrons, injected from the cathode 1 into QB-semiconductor 2 through the surface S2, travel along the quasi-ballistic trajectories within the QB-semiconductor. They emerge, through the surface S3 and enter either the patterned absorbing template 19 or the anode 4. The part of the quasi-ballistic electrons, not stopped by the electron absorbing template 19, then have enough energy to enter the free space FS through the surface S4 as for example the electron at point i. These electrons are then accelerated within the free space region, FS, to sufficiently high energies by the electron acceleration electrode 7. The electron acceleration electrode 7 consists in this particular illustration of the wafer and the deposited electron sensitive resist 6.

Through electron-optical means, the electrons that emerge for example at point i (Figure 10) are imaged into point j, lying within the resist layer 6. In this way the entire lithographic pattern (layer 19) can be transferred onto the said wafer - resist assembly at once and not sequentially as is the case with the standard Electron Beam Lithographers. Also, there are no principal limits on the lateral dimensions of the patterned layer 19 and this means that the entire wafer can be processed in one exposure. The minimum feature obtainable ("MinS") lies well below 0.15 micron, if the electron-optical system, together with the planar electron emitter part of the electron 1: 1 projection stepper is optimised. Furthermore, by exposing the whole wafer at once, the throughput of such a planar electron beam

lithographic system is very large. A number of other arrangements of planar electron lithographer are possible, an arrangement shown in Figure 10 being just one of them.

One of possible alternatives to the embodiment shown in Figure 10 is shown in Figure 9. Referring to Figure 9 now, the same basic quasi-ballistic electron emitter structure, as discussed in reference to Figure 10, is clearly apparent. In the particular preferred embodiment shown in Figure 9, an accelerating electrode 7 and electron scintillator 17 structure has been inserted between the planar electron emitter structure 1, 2, 19, 4 and wafer plus photo-resist part 6. Such an arrangement allows for the planar electron projection system to be under vacuum (it is the region 17, 12 and 14 that form the vacuum encapsulation of the said electron emitter structure), operating continuously if necessary, while the wafers to be processed can be placed on the top of the scintillator 17. Operating in vacuum gives a better electron transmission from the emitting surface to the wafer, and without a need for prior evacuation, the throughput of the whole device is increased. If the air space, indicated in Figure 9 is sufficiently small, the degradation of the size of the minimum feature "Min" due to optical spreading can be kept to minimum.

In the publication by some of the inventors of the present invention mentioned in the prior art (H. Ahmed et al.: "Proceedings of the Conference on Microlithography"; Cavendish Laboratory, Cambridge 1989), it is shown and demonstrated experimentally in Figures 11, 12, 13 and 14 how to carry out Planar Electron Beam Lithography in practice. An apparatus - "Experimental 1: 1 Electron Projection Stepper" is disclosed and its performance that met all the industrial needs and requirements concerning the necessary lithographic steps during IC production has been clearly demonstrated. Its schematic diagram is shown in Figure 11. Here 20 is the said cathode - QB-Sem - anode assembly (very similar in construction to the arrangement shown in Figure 10 - parts 1, 2, 19 and 4), 6 is the wafer substrate with the deposited resist layer, 21 is the x, y positioning table and finally 22 is a pair of Helmholtz coils to generate a homogeneous magnetic field between the cathode - anode assembly and the wafer - x,y table assembly. In this particular arrangement, it is the cathode - QB-Sem - anode assembly that was negatively biased with the respect to the wafer substrate that was kept near ground potential. The emitted electrons have been accelerated in the established electrical field from high negative potential towards ground. The parallel electrical and magnetic fields formed in this way an electron - optical 1: 1 projection system that transferred the electrons emerging from a particular point on the

bottom surface of the cathode - QB-Sem - anode assembly 20 to a single point within the resist layer 6 (see also Figure 10).

The over-all view of the said experimental 1: 1 electron projection stepper is shown in Figure 12 and some typical experimental results of wafer patterning in Figures 13 and 14. Both positive and negative resists were tested and with typical exposure times of the order of 0.1 seconds, the minimum features easily attainable (length "Min" in Figure 8) were in the region of 0.15 microns (Figures 13 and 14). While a part of the whole, exposed and patterned (repetition of test patterns) silicon substrate is shown in Figure 13, the structural details of the test patterns are shown in Figure 14, clearly demonstrating the 0.15 micron minimum feature capability of this prototype instrument.

Example 3. Two-dimensional illumination panels

Due to the simplicity of design, robustness, low power dissipation, low temperature operation and two-dimensional nature of the planar electron emitter according to the present invention, the said planar electron emitter can be used very conveniently in the construction of two-dimensional (planar and non-planar) illumination sources.

One such possible flat illumination panel is shown schematically in Figure 15 and 16. Here the basic structure of the planar electron emitter (cathode 1, QB-semiconductor 2 and the anode 4) is used as planar source of electrons (when an appropriate electrical voltage is applied between the cathode and the anode) emerging into the free space FS. These electrons are accelerated within this space by means of the accelerating electrode 7 and enter the light emitting layer 3. The optically transparent plate 13 (typically a glass plate) that allows the generated light to escape from the said structure forms (together with plates 14 and 12) the vacuum encapsulation of the whole assembly.

In another possible arrangement, the light emitting layer 3 is left out and the free space FS is filled with an appropriate gas and/or gas mixture, the necessary illumination being now generated through gas ionisation and fluorescence. The typical dimensions of the above-described flat illumination are indicated in Figure 16. While "Dim1" - the thickness of the illumination panel can be easily under one centimetre; the "Dim2" can be easily of the order of meters.

Because of the simplicity of construction, the present invention can be used also in the construction of non-planar (round) two-dimensional illumination sources. One of the possible arrangements of such a source is shown schematically in Figure 17. Here, the cathode 1, the QB-semiconductor 2 and the anode 4 are concentric cylindrical layers. The QB electrons emerge into the free space FS radially and after acceleration via accelerating electrode 7, they enter the light emitting region 3. The generated light escapes through the transparent (glass) envelope 13. Also in this arrangement, the light emitting layer 3 can be left out and the free space can be filled with the appropriate light emitting gas.

Example 4. Semiconductor components and devices

In what follows, only a brief description of some typical applications of the present invention within the field of semiconductor components, devices and Integrated Circuits' manufacture will be given and these must be considered only as few illustrative examples and in no way should they represent a limiting factor as far as the use of the present invention within this field is concerned. The examples to be shown, have been chosen from four different major classes (A to D) of semiconducting components/devices where the present invention can be used:

In these examples, the basic structure (the cathode, QB-semiconductor and the anode) of the present invention is preserved, although in some applications only the properties of quasi-ballistic electrons between the two electrodes are utilised, rather than their ability to escape into free space FS (see Figure 2). The names "cathode" and "anode" will not always be used now in attempt to use more the terminology of Semiconductor Physics. These electron transmitting properties of the QB-Semiconductor are very similar to the properties of electrons moving between a cathode and an anode in a vacuum tube, only now no vacuum is needed. The injection of electrons from the cathode takes place at room temperature and the whole device in question can be made of submicron dimensions. In this way the present invention combines all the advantages of vacuum tubes and modern all solid state semiconductor technology.

Example 4a

Class A: Rectification and charge (information) storage

Semiconductor components/devices in this class include bipolar p - n, p - i - n diodes, thyristors as well as a number of unipolar devices such as MIS (Metal - Insulator - Semiconductor) diodes, CCD (Charge Coupled Device), MIS tunnel diodes, MIS switch diodes, IMPATT (Impact Ionisation Avalanche Transit Time) and BARITT (Barrier Injection and Transit Time) diodes and other related Transit Time devices.

Example: Quasi-ballistic Schottky diode.
Figure 18 is a schematic diagram of a typical, fast, planar Schottky barrier diode according to the present invention. Also displayed are the equivalent R, C electrical networks 36 and 37 (see US 5,627,479 and EP 672 257 B1), describing the electrical response of a prior art diode 36 and a QB-Semiconductor diode 37.

In reference to Figure 18 now, the diode current I_{diode} is controlled by the depletion resistance Rd which is in turn determined by the extend of the depletion region W_d. This depletion region length (width) W_d is exponentially dependent on the applied voltage V_{so} between the Schottky and Ohmic electrical contacts. The rectification action is achieved through the control of W_d by V_{so}, which in turn induces exponentially strong changes in Rd that controls the diode current I_{diode} (forward and reverse diode current). Since there is no electron velocity saturation at high electrical fields, it is not necessary to diminish the overall dimension L, and in particular the distance L_{so} between the front of the depletion region and the ohmic contact, in high frequency applications. The Quasi-ballistic Schottky diode according to the present invention will be workable at higher frequencies and will be characterised by simpler design and very low power dissipation through shunting of the resistor R_{qb} by L_{qb} (quasi-ballistic electrons' kinetic inductance) in 37 of Figure 18.

Example 4b
Class B: Photo-Sensing and Photo-Emitting devices

This class of semiconducting components/devices include among others LEDs' (Light Emitting Diodes), Photodiodes, Semiconducting Lasers, Avalanche diodes and other photoconducting devices for light to electrical signal conversion purposes.

Example: Quasi-ballistic Photodiode and Quasi-ballistic Light emitting diode.
A simplified energy band diagram shown in Figure 19 illustrates the physical principles behind and one possible construction (preferred embodiment) of a quasi-ballistic

photodiode (A - references), a quasi-ballistic Light-Emitting diode (B - references) and one of the possible constructions (preferred embodiment) of a first stage of an optical signal detection/amplification/spatial magnification device (C - references), all according to the present invention These devices will be now discussed in turn.

Quasi-ballistic photodiode (process A in Figure 19).
The optical signal (incoming light) is absorbed within the cathode region (region between the surfaces S1 and S2 - Figure 19) and a thin region within the QB-semiconductor that lies close to the surface S2, creating in this process a number of electron - hole pairs (process marked "Exc1" in Figure 19). The photo-excited electrons then constitute the quasi-ballistic current Ibal, are accelerated and enter the avalanche multiplication region AMR through the surface S5. The avalanche multiplication process AM leads to an amplified electrical current signal I_e and I_h. In some applications the avalanche multiplication region AMR can be left out, the electrical signal from the photon - electron conversion ("Exc1") being sufficiently amplified through the acceleration of the generated quasi-ballistic electrons.

The described quasi-ballistic photodiode according to the present invention has high quantum efficiency, relatively very low power dissipation and can be manufactured in a form of two-dimensional photo-sensor array when two-dimensional optical image (signal) detection and processing is required.

Quasi-ballistic Light-Emitting Diode (process B in Figure 19).
In the case of Light-Emitting device, the electrical signal (voltage bias between the cathode and the anode) that can be also time modulated if needed (opto-electronic applications), controls the amount of injected electrons that enter the QB-semiconductor region QB-S_{em} (process "Exc2" in Figure 19). After acceleration, while moving through the QB-Sem region, these electrons (current I_{bal} in Figure 19) enter the Light Emitting Region (LER) through the surface S5 and create photon flux through the process of recombination across the band gap E_g (see Figure 2 and process B in Figure 19). This photon flux (that is also time modulated if the cathode - anode voltage bias ~ ΔQ (t) is time dependent) then finally emerges into the free space FS.

When the electron injection process "Exc2" is of sufficient intensity and the light emitting region LER (normally heavily p-doped) satisfies the necessary conditions for population inversion, the above described device will function as a quasi-ballistic semiconductor laser

with a very low power dissipation, high efficiency and can be used very effectively in opto-electronic applications such as optical fibre signal transmission and tele-communications in general.

Optical image detection and processing (process C in Figure 19).
In some applications it will be necessary and/or advantageous to process the quasi-ballistic current I_{bal}, formed either through process "Exc1" and/or through process "Exc2", electron - optically. In this case the region between the interface S5 and S3 is just a continuation of the quasi-ballistic semiconductor region QB-Sem as shown in Figure 19. After traversing the anode region, these quasi-ballistic electrons emerge through the surface S4 into the free space FS as the electron emission current I_{em} that can be now processed electron - optically. A device of this type will described in Example 4d.

Example 4c
Class C: Amplification and Non-volatile memory

Applications of the present invention in this class of semiconductor components/devices include also bipolar transistors and bipolar unijunction transistors, together with a number of unipolar components and devices inclusive FETs (Field Effect Transistor), JFETs (Junction Field Effect Transistor), MESFETs (Metal - Semiconductor Field Effect Transistor), MOSFETs (Metal - Oxide - Semiconductor Field Effect Transistor) and Non-Volatile Memory devices. Particularly relevant in relation to present invention within this class are tunnel transistors, TEDs (Transferred - Electron Devices) and other ballistic (Hot Electron) transistors and/or devices.

Example: Quasi-ballistic Transistor.
Figure 20 is a schematic diagram of a typical planar Metal - Semiconductor Field Effect Transistor (MESFET). The current I_d between the source and the drain electrodes is controlled by the voltage V_g through changing the active depletion width W_d (V_d). "a" is the electrically active part of the substrate semiconductor SEM, "L" is the conductivity channel length and "Z" is the width of the device. When a high-speed performance is required, the channel length has to sufficiently reduced (< 1.5 micron) and the typical operating voltages V_{ds} create high electrical fields between the source and the drain. The velocity of electrical charges (electrons) becomes then saturated (electrical field dependent mobility region is reached) and this limits the speed of the said device operation.

Now, even if the geometrical design of the said MESFET transistor as shown in Figure 20 is kept the same for the sake of simplicity and clarity of the argument, the two above mentioned design constraints (small geometry and electron velocity saturation) are non-existent, when such a MESFET transistor is constructed according to the present invention. Given the form of the device as shown in Figure 20, this involves simple replacement of the standard semiconductor substrate Sem (see Figure 20) by the quasi-ballistic semiconductor QB-Sem.

MESFET device according to the present invention and depicted in Figure 20 is characterised not only by fast response (high frequency response), but also by very low power dissipation since source-drain current Id is quasi-ballistic in nature.

It has to stressed at this point again that the design structure of MESFET transistor shown in Figure 20 is only one of a large number of possible designs of an amplification / switching device. Due to the nature of the present invention, other more optimal designs are possible and will be realised. These will take over some design features from vacuum tubes (see for example the above-mentioned publication by K.W. Boer: p.1237).

The same and/or very similar arguments as discussed above for the case of MESFET transistor lie behind the construction of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), Non-Volatile memory MOSFETs and other devices within this class according to the present invention All of these devices are characterised by simplicity of design, robustness, high response speed and very low power dissipation.

Example 4d

Class D: Optical image detection, formation and processing

Due to two-dimensional nature of the present invention, large areas optical signal detection, conversion and processing is possible. Taking electromagnetic radiation as an example, the present invention can be used in a number of ways:

- Conversion of recorded electrical signals (electrically recorded optical images) back to two-dimensional images/signals (Quasi-ballistic semiconductor Field-Emission Flat Panel Display - see also Example 1).

- Conversion of two-dimensional optical images to electrical signals (Quasi-ballistic semiconductor camera)
- Two-dimensional optical image detection, the resulting electrical signal amplification, followed by two-dimensional optical image spatial magnification and final two-dimensional optical image recording. The result of this type of optical image processing is the original two-dimensional optical image, but now contrast/intensity amplified and spatially magnified.

The two last ways are both two-dimensional detector arrays of electromagnetic radiation to be used in optical image detection, formation and processing. This involves what could be roughly defined as two basic applications of the present invention:

a) Quasi-ballistic semiconductor camera (Conversion of 2D-optical images/signals to electrical signal sequences)
b) A system for 2D-optical image/signal brightness/contrast amplification and spatial magnification

In this paragraph a short description of QB-semiconductor camera a) and of optical image/signal processing system b) will be described. For the sake of clarity and simplicity, the two applications will be described assuming the optical signal to be in the form of two-dimensional optical image formed by the photons from within the visible part of the electromagnetic radiation spectrum. This of course must not be considered in any way as a limiting factor in relation to the present invention and its use within this class of applications. The optical signal to be detected/processed may well be from within other parts of the electromagnetic radiation spectrum and/or it may be a signal formed by other particles. The optical image spatial dimension can also vary from zero to three. Finally, the specificity of the two application examples of the present invention to be presented below, serves purely illustrative/pedagogical purposes and must not be considered either as a limiting factor in relation to the applications of the present invention within this field.

a) Quasi-ballistic semiconductor camera.

Figure 21 is a schematic diagram of a device according to the present invention for the detection and recording of two-dimensional optical signals/images. In this preferred embodiment the QB-semiconductor is sandwiched between a cathode 1 and an anode 4. Both electrodes are patterned in a way similar to x, y patterning shown in Figure 5. The metal cathode, QB-semiconductor and the anode form a two-dimensional array of Schottky

barrier photodiodes that can be addressed individually and sequentially, as illustrated in Figure 5 (pixel diode i, j - switched on).

The optical image is formed at around the surface S2 and is transformed and processed, with help of the said device, to time sequence of electrical signals in the following way: Optical image forming light (photons) enters the said structure shown in Figure 21 through appropriate colour filters R (red), Y (yellow) and B (blue) and it is absorbed within the region consisting of cathode - QB-semiconductor interface and QB-semiconductor depletion region, creating in this process a number of electron - hole pairs.

By "switching-on" a particular pixel diode (i, j) by applying an appropriate electrical voltage between a cathode strip "i" and an anode strip "j" (diode with yellow colour filter "Y" in Figure 21), the created quasi-ballistic electrons are accelerated within the QB-semiconductor region QB-S_{em} (Figure 21) and if needed can be amplified further by avalanche multiplication within the avalanche multiplication region AMR (Figure 21). The resulting current pulse then forms the electrical signal which is related to the light intensity of "yellow" photons impinging on the pixel (i, j) shown in Figure 21.

The overall thickness (Dim2) of the said device (QB-semiconductor camera) is in the region of few millimetres, while the active area of the said device (lateral dimension Dim1) can be of the order of up to some 30 centimetres with the present day technology. High quantum efficiency, high spatial resolution, robustness and the simplicity of construction are just few of the attractive features of the proposed device according to the present invention.

b) Optical signal/image processing device.
In a number of applications (such as astrophysics, infra-red vision/imaging and others), very weak, two-dimensional optical images have to be detected, processed and recorded, with an additional demand for high spatial resolution/magnification and/or for spectral information to be extractable. One of possible devices according to the present invention that fulfils these requirements is shown schematically in Figure 22. It consists of two parts, where part A is the two-dimensional optical image/signal amplification part, while the part B is the two-dimensional optical image/signal spatial magnification part.

The incoming photons that forms the optical image in the plane of the primary optical image 25 is absorbed within the region of the cathode, interface S2 and the depletion

region of the QB-semiconductor as indicated schematically in Figure 22, creating in this way a number of electron - hole pairs. This number depends both on the energy of incoming photons (spectroscopic information) and on the number of incoming photons (the signal intensity information). The quasi-ballistic electrons created within the plane of the primary optical image are accelerated within the QB-semiconductor region QB-Sem (primary amplification) and because of their properties they can leave the basic planar electron emitter structure (cathode, QB-semiconductor and the anode) through the surface S4. At the same time though they form in this way also an electron - optical image of the original optical image in the plane of the primary optical image.

After this photon to electron conversion (photon in - electron-hole pair out) and primary amplification (acceleration of the created electrons within QB-Sem region), the obtained electron-optical image formed in the plane of the surface S4 can be processed further by suitable electron optics (not shown). It is further amplified with the help of the accelerating electrode (secondary amplification) and can be if needed spatially magnified (electron-optical primary spatial magnification).

This spatially magnified and intensity amplified electron-optical image is converted back to a second stage optical image with the help of an appropriate electron scintilator 17. The plane 26 of this second stage optical image then becomes the object plane of the final optical magnification system 29 to secure the secondary spatial magnification of the original optical image. The final optical image, that is signal/intensity amplified in part A and spatially magnified in 29 is then formed in the plane 27 of the final optical image ready for recording by a proper optical recording device 28 (photographic plate or CCD). Depending on the spatial resolution required the whole assembly (part A and part B) can be moved laterally within the plane of the primary optical image.

Finally it should be pointed out that because of the characteristic properties of the basic planar electron emitter that forms the bottom portion of the part A of the device, the said planar electron emitter in conjunction with the electron-optical parts within the free space region FS can be used as a spectroscopic device, extracting the necessary information about the photon energy spectrum within the primary optical image.

Example 5. Photovoltaic applications

Due to very low inelastic scattering and recombination rates of the quasi-ballistic electrons, a Schottky barrier diode according to the present invention is a highly efficient photoconductor and its use in the photovoltaic applications is obvious. One of the possible constructions of a solar cell according to the present invention is shown schematically in Figure 23.

The said device is formed by QB-semiconductor layer 2 sandwiched between two electrodes - a cathode 1 and an anode 2. While the cathode and the QB-semiconductor form a Schottky rectifying contact, the anode and the QB-semiconductor form an ohmic contact. When constructed in this way (using a p-type QB-Sem), the internal electrical field E(x) within the said device, caused by the electrical charge transfer that takes place in order to establish thermodynamical equilibrium, has a profile shown in the bottom part of Figure 23.

The sunlight enters the said device (solar cell according to the present invention) from the left (Figure 23) through the cathode and is absorbed within the structure, creating single electron-hole pair per incoming photon. Three, spatially separated absorption processes can be distinguished. The process D is the generation of electron-hole pair at the interface between the cathode and the QB-semiconductor. The process E is a generation of electron-hole pair within the depletion region of the QB-semiconductor and finally the process F describes the photon absorption process generating electron-hole pair within the bulk of the QB-semiconductor (region of QB-Sem where the internal electrical field is zero). Due to the existence of quasi-ballistic trajectories within the QB-semiconductor a majority of electrons generated especially within the depletion region of the QB-semiconductor will be accelerated by the internal electrical field existing within the depletion region W_d towards the anode without recombination and/or inelastic scattering. This effect increases appreciably the quantum efficiency of the said solar cell. By optimising the structure of the said device through minimising the extend of the bulk region and through an appropriate choice of the cathode material (transparent conducting tin oxide for example), the solar cell according to the present invention represents a very efficient, simple and robust light to electricity energy conversion device with a large active area.

Example 6. Electron Cold Emission Microscopy

There is a potentially very important application of the present invention within the field of defects and/or imperfections investigations in the "virgin" semiconductor wafers by what is termed here as Electron Cold Emission Microscopy (ECEM). This is discussed in relation to Figure 24.

In the standard version of the Electron Emission Microscopy, a sample to be investigated is heated up to temperatures when the thermal electron emission becomes finite. These electrons leave the sample through a surface and are subsequently electron-optically processed to form a high spatial resolution electron optical image of that fraction of the surface through which they emerged into the vacuum. However, the information about the sample under investigation that can be extracted from such type of electron microscopy is limited to the surface and few monolayers of the material right below it. This is because under these conditions the mean free path of the electrons (with sufficient energies to escape into vacuum) is extremely small (well below some 50 Angstroms).

In the proposed version of this experimental method according to the present invention, the electrons that leave the sample (QB-Sem region in Figure 24) through the surface S3, have been injected to the said QB-semiconductor already at the surface S2 and therefore they carry the information about the conditions of the sample along the whole of their quasi-ballistic trajectory within the sample. Any imperfections and/or defects (these may be of one, two and/or three - dimensional variety) will cause their scattering (and their subsequent thermalising) away from their quasi-ballistic straight trajectories. This creates a projection-type of contrast in the electron-optical image plane.

One of the possible preferred embodiments of the said Electron Cold Emission Microscopy according to the present invention is shown schematically in Figure 24. The basic structure of the present invention (cathode, QB-semiconductor, anode - see also Figures 1 and 2) is preserved also in this case, only now the said basic structure forms a sample to be investigated. Furthermore the metal electrodes facing the QB-semiconductor surface S2 and S3 are not really necessary, provided that the electrical field of sufficient strength can be generated within QB-semiconductor body and the electrons can be injected into the QB-semiconductor through the surface S2. In such configuration the whole process of virgin defect quality control can be performed contactless. These injected electrons travel along their straight, quasi-ballistic trajectories and those not deflected by imperfections, impurities, defects and/or other irregularities, will eventually emerge into vacuum through

the surface S3 of the QB-semiconductor. The surface density of these electrons, their energies and the angle of their emergence are the parameters (quantities) that are related to the precise quasi-ballistic electrons' interaction with the surface S2, with the bulk of the QB-semiconductor along their trajectory and with the surface S3.

The electrons emerging through the segment 32 of the surface S4 are then processed by standard electron optics 34 to form high spatial resolution (magnified) electron-optical image 33 of the said segment in the electron-optical image plane 30

By placing the QB-semiconductor on a high precision x, y stage, the whole wafer can be investigated in this way down to 10 to 50 Angstroms standard resolution of a typical scanning electron microscope.

Example 7. Electron beam sources in general

Although the present invention (planar electron emitter) is primarily targeted towards applications that require and/or benefit from the two-dimensional nature of the said invention, the present invention characteristics (such as low power dissipation, simplicity of construction, high electron emission current density and room temperature operation) make the use of the present invention in the construction of more standard electron beam sources also very attractive. Pointed, patterned, quasi-planar and general shape electron sources can be manufactured with ease and are termed here as "Cold Schottky Cathodes". Their typical use will be as electron sources for Cathode Ray Tubes (CRT), x-ray tubes, Electron microscopes inclusive electron guns for evaporation, welding, imaging and possibly other electron beam applications.

Since all these applications are considered as trivial use of the present invention and because they are well known and described in the corresponding prior art, they will not be discussed here in more detail.

CLAIMS

1. An article comprising

- an element having a first and a second surface, wherein

  - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, the first surface being substantially parallel to the second surface, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- means for providing an electric field across at least part of the element, said means comprising

  - means for providing the first electrical charge to the first surface of the element, and

  - means for providing the second electrical charge to the second surface of the element, the second electrical charge being different from the first electrical charge in order to move electrons in a direction substantially perpendicular to the first or the second surface.

2. An article according to claim 1, wherein the material or material system comprises a semiconductor material, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

3. An article according to claim 1 or 2, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

4. An article according to claim 3, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

5. An article according to claim 3, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

6. An article according to any of claims 1-5, wherein the means for providing the first electrical charge to the first surface comprises an at least partly conductive first material or material system.

7. An article according to any of claims 1-5, wherein the means for providing the second electrical charge to the second surface comprises an at least partly conductive second material or material system.

8. An article according to claim 6, wherein the at least partly conductive first material or material system constitutes a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element.

9. An article according to claim 7, wherein the at least partly conductive second material or material system constitutes a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

10. An article according to any of claims 6-9, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor material with a doping level higher than $1x10^{17}$ cm^{-3}.

11. An article according to claim 10, wherein the at least partly conductive first and second material or material system comprises gold, chromium, platinum, aluminium, copper, cesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

12. An article according to any of claims 1-11, wherein the electrons comprise quasi-ballistic electrons.

13. A method for providing a first type of electrons, said method comprising the steps of:

- providing an element having a first and a second surface, wherein

  - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, the first surface being substantially parallel to the second surface, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- providing means for providing the first electrical charge to the first surface of the element, and

- providing means for providing the second electrical charge to the second surface of the element, the second electrical charge being different from the first electrical charge so as to move a second type of electrons in a direction substantially perpendicular to the first or second surface.

14. A method according to claim 13, wherein the material or material system comprises a semiconductor material, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

15. A method according to claim 13 or 14, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

16. A method according to claim 15, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

17. A method according to claim 15, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3},.such as less than $1x10^{12}$ cm^{-3}.

18. A method according to any of claims 13-17, wherein the means for providing the first electrical charge to the first surface comprises an at least partly conductive first material or material system.

19. A method according to any of claims 13-17, wherein the means for providing the second electrical charge to the second surface comprises an at least partly conductive second material or material system.

20. A method according to claim 18, wherein the at least partly conductive first material or material system constitutes a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element.

21. A method according to claim 19, wherein the at least partly conductive second material or material system constitutes a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

22. A method according to claim 20 or 21, wherein a potential difference between the first and second terminals of the charge reservoir is larger than 2 volts.

23. A method according to any of claims 18-21, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor material with a doping level higher than $1x10^{17}$ cm^{-3}.

24. A method according to claim 23, wherein the at least partly conductive first and second material or material system comprises gold, chromium, platinum, aluminium, copper, cesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

25. A method according to any of claims 13-24, wherein the second type of electrons comprises quasi-ballistic electrons.

26. A method for fabricating an article, said method comprising the steps of:

- providing a semiconductor material or material system having a first and a second surface, the second surface being substantially parallel to the first surface, the semiconductor material or material system having a predetermined crystal orientation perpendicular to the first or second surface,

- providing a surface treatment to the first and second surfaces so as to reduce surface roughness,

- doping the semiconductor material or material system with a dopant so as to obtain a predetermined doping level so as to reduce electron scattering within the material or material system,

- providing an at least partly conductive first material or material system, said first material or material system forming a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element, and

- providing an at least partly conductive second material or material system, said second material or material system forming a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

27. A method according to claim 26, wherein the semiconductor material comprises silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

28. A method according to claim 26 or 27, wherein the predetermined crystal orientation is the <111>, <110> or <100> direction.

29. A method according to any of claims 26-28, wherein the surface treatment comprising optical polishing.

30. A method according to any of claims 26-29, wherein the dopant comprises lithium, phosphorus, antimony, arsenic, boron, aluminium, tantalum, gallium or indium or any combination thereof.

31. A method according to any of claims 26-30, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

32. A method according to any of claims 26-31, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor material with a doping level larger than $1x10^{17}$ cm^{-3}.

33. A method according to claim 32, wherein the at least partly conductive first and second material or material system comprises gold, platinum, chromium, aluminium or copper or any combination thereof.

34. A flat panel display comprising

- an article according to any of claims 1-12, the article further comprising

- a layer of material being adapted to emit light at a plurality of wavelengths upon exposure of electrons, said material layer defining, in a plane substantially parallel to the first and second surface of the element, a two-dimensional matrix having one or more surface elements, each surface element being adapted to emit light at a predetermined wavelength, and

- means for selectively proving electrons to the one or more surface elements in the two-dimensional matrix.

35. A flat panel display according to claim 34, wherein the material layer for emitting the plurality of wavelengths comprise an appropriate luminophors or standard colour television phosphors.

36. A flat panel display according to claim 34 or 35, wherein the emitted light comprises at least three wavelengths corresponding to at least three colours.

37. A flat panel display according to claim 36, wherein any colour may be deduced from a combination of the at least three colours emitted from the layer.

38. A flat panel display according to any of claims 34-37, wherein the emitted wavelengths corresponds to colours red, yellow and blue, or to colours red, green and blue.

39. A flat panel display according to any of claims 34-38, wherein the electrons comprise quasi-ballistic electrons.

40. A flat panel display according to any of claims 34-39, wherein the selective means comprises a pattern so as to define, in a plane substantially parallel to the first or second surface, a two-dimensional matrix of electrically controllable matrix

elements, said pattern being formed of the at least partly conductive material or material system.

41. A method for exposing a film to a plurality of electrons of a first type, said method comprising the steps of:

- providing a first element having a first and a second surface, wherein

  - the first surface is adapted to hold a first electrical charge, and wherein the second surface is adapted to hold a second electrical charge, and wherein

  - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- providing a second element, said second element being adapted to hold the film to be exposed to the plurality of electrons of the first type,

- providing a patterned absorption layer, said absorption layer being adapted to absorb electrons transmitted through the first element at positions determined by the pattern,

- providing the first electrical charge to the first surface of the first element, and

- providing the second electrical charge to the second surface of the first element, the second electrical charge being of opposite sign compared to the first electrical charge so as to move a second type of electrons from the first surface towards the second surface, and

- providing a third electrical charge to the second element, said third electrical charge having the same sign as the second electrical charge.

42. A method according to claim 41, wherein the material or material system

comprises a semiconductor material, such as silicon, germanium, silicon carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

43. A method according to claim 41 or 42, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

44. A method according to claim 43, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

45. A method according to claim 43, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

46. A method according to any of claims 41-45, wherein the first electrical charge is provided to the first surface of the first element from a first terminal of a charge reservoir.

47. A method according to any of claims 41-45, wherein the second electrical charge is provided to the second surface of the first element from a second terminal of the charge reservoir.

48. A method according to any of claims 41-44, wherein the third electrical charge is provided to the second element from a third terminal of the charge reservoir.

49. A method according to claim 46 or 47, wherein a potential difference between the first and second terminals of the charge reservoir is larger than 2 volts.

50. A method according to any of claims 41-49, wherein the second element comprises a metal or a semiconductor material, such as silicon, germanium, silicon

carbide, gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

51. A method according to any of claims 41-50, wherein the film comprises a resist.

52. A method according to any of claims 41-51, wherein the second type of electrons comprises quasi-ballistic electrons.

53. An article comprising

- an element having a first and a second surface area, wherein

    - the first surface area is adapted to hold a first electrical charge, and wherein the second surface area is adapted to hold a second electrical charge, and wherein

    - the element comprises a material or a material system being prepared so as to reduce electron scattering within the material or material system, and having a predetermined crystal orientation perpendicular to the first or second surface,

- means for providing an electric field across at least part of the element, said means comprising

    - means for providing the first electrical charge to the first surface area of the element, and

    - means for providing the second electrical charge to the second surface area of the element, the second electrical charge being different from the first electrical charge in order to move electrons between the first surface area and the second surface area.

54. An article according to claim 53, wherein the material or material system comprises a semiconductor material, such as silicon, germanium, silicon carbide,

gallium arsenide, indium phosphide, indium antimonide, indium arsenide, aluminium arsenide, zinc telluride or silicon nitride or any combination thereof.

55. An article according to claim 53 or 54, wherein the preparation of the material or material system comprises doping the material or material system with a dopant so as to obtain a predetermined doping level.

56. An article according to claim 55, wherein the dopant comprises phosphorus, lithium, antimony, arsenic, boron, aluminium, tantalum, gallium, indium, bismuth, silicon, germanium, sulfur, tin, tellurium, selenium, carbon, beryllium, magnesium, zinc or cadmium or any combination thereof.

57. An article according to claim 55, wherein the predetermined doping level is less than $1x10^{18}$ cm^{-3}, such as less than $1x10^{16}$ cm^{-3}, such as less than $1x10^{14}$ cm^{-3}, such as less than $1x10^{13}$ cm^{-3}, such as less than $1x10^{12}$ cm^{-3}.

58. An article according to any of claims 53-57, wherein the means for providing the first electrical charge to the first surface comprises an at least partly conductive first material or material system.

59. An article according to any of claims 53-57, wherein the means for providing the second electrical charge to the second surface comprises an at least partly conductive second material or material system.

60. An article according to claim 58, wherein the at least partly conductive first material or material system constitutes a layer having a first and a second surface, wherein the second surface is operationally connected to a first terminal of a charge reservoir and wherein the first surface is in direct contact with the first surface of the material or material system of the element.

61. An article according to claim 59, wherein the at least partly conductive second material or material system constitutes a layer having a first and a second surface, wherein the first surface is operationally connected to a second terminal of the charge

reservoir and wherein the second surface is in direct contact with the second surface of the material or material system of the element.

62. An article according to any of claims 57-60, wherein the at least partly conductive first and second material or material system comprises a metal or a highly doped semiconductor with a doping level higher than $1x10^{17}$ cm^{-3}.

63. An article according to claim 61, wherein the at least partly conductive first and second material or material system comprises gold, chromium, platinum, aluminium, copper, cesium, rubidium, strontium, indium, praseodymium, samarium, ytterbium, francium or europium or any combination thereof.

64. An article according to any of claims 53-63, wherein the electrons comprise quasi-ballistic electrons.

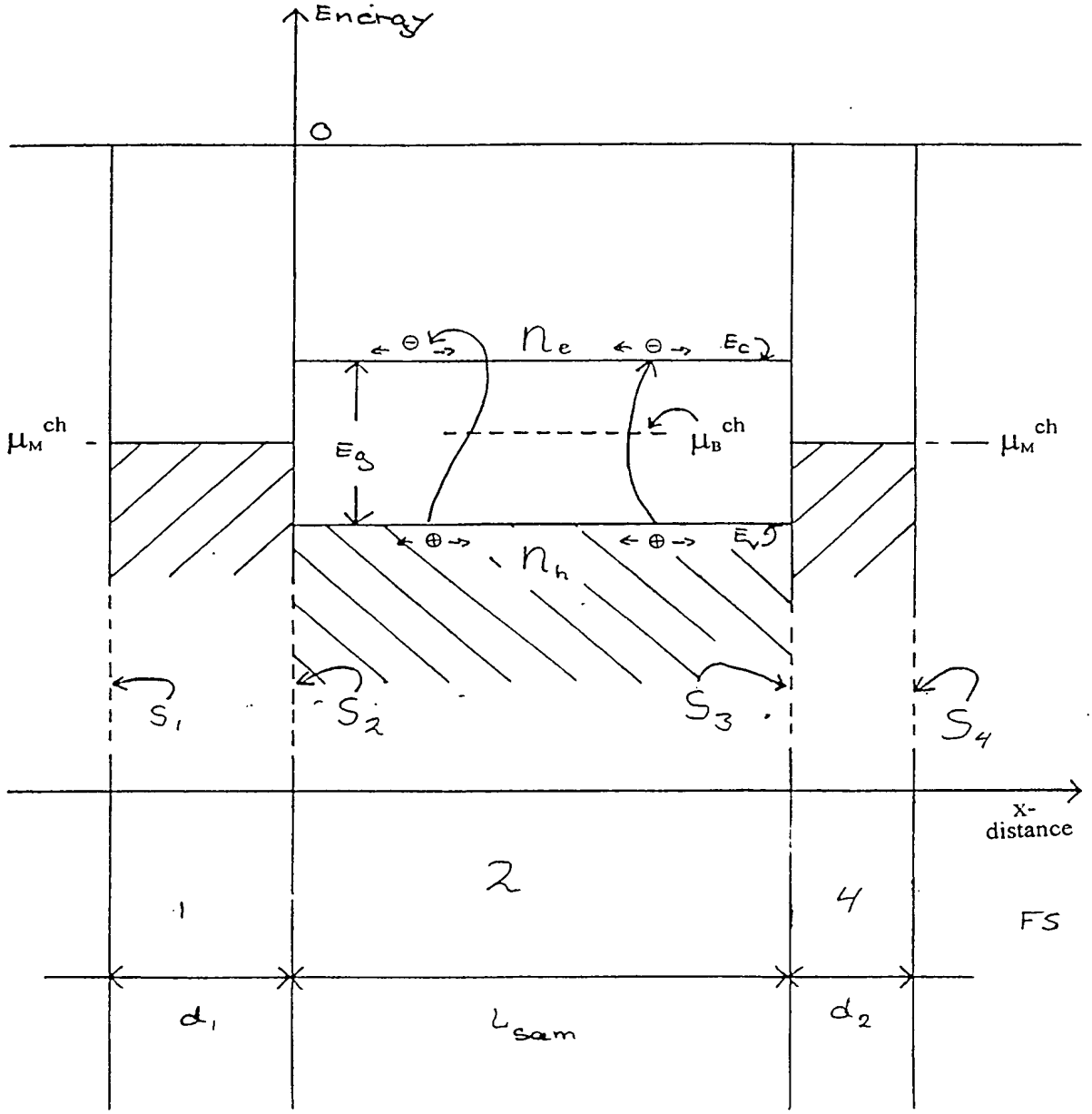
Energy
0
n_e
E_c
μ_M^{ch}
E_g
μ_B^{ch}
μ_M^{ch}
E_v
n_h
S_1
S_2
S_3
S_4
x-distance
1
2
4
FS
d_1
L_{sam}
d_2

Fig. 1

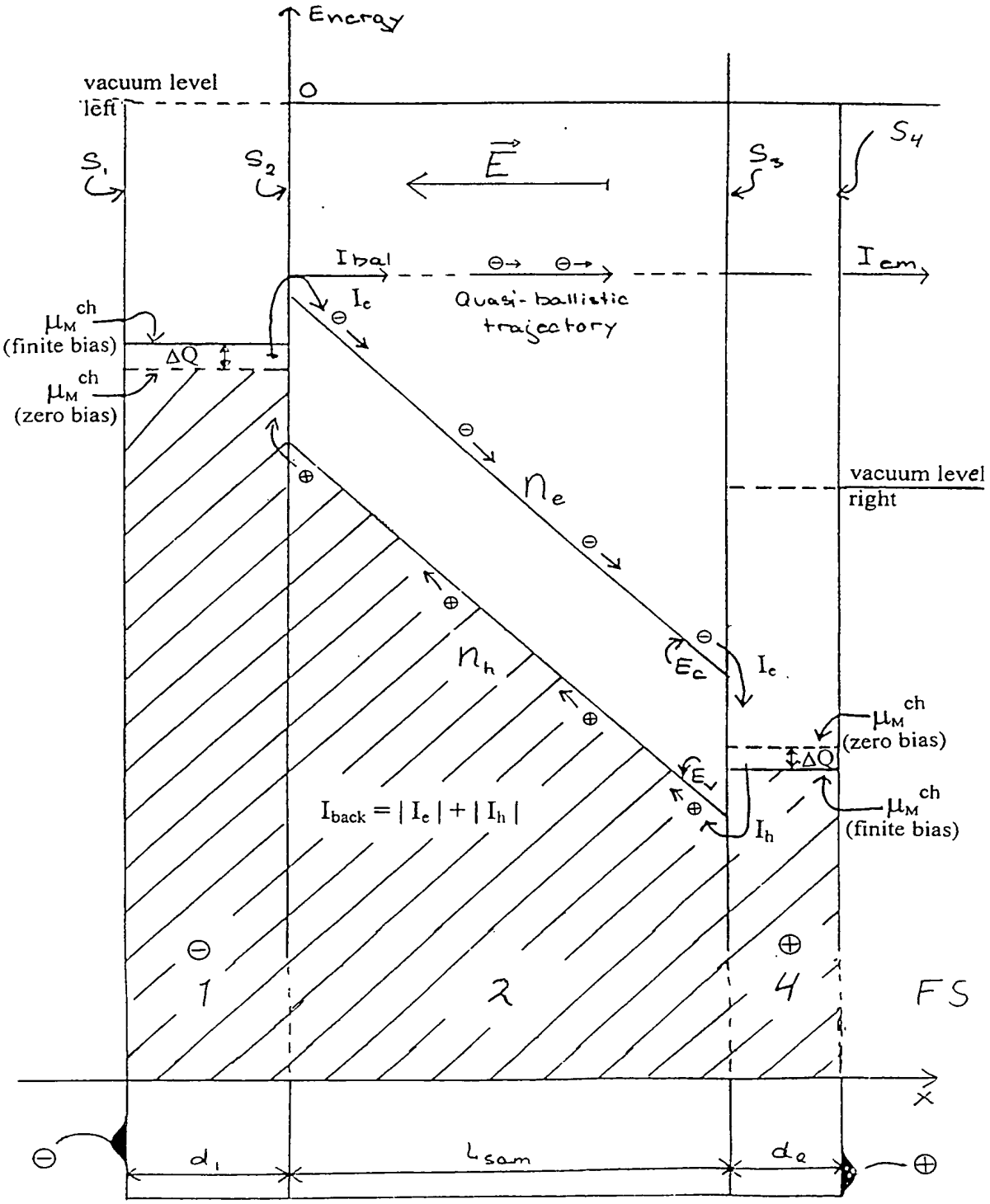
Energy
vacuum level
left
0
S_1
S_2
$\vec{E}$
S_3
S_4
I_{bal}
I_{em}
Quasi-ballistic
trajectory
I_c
μ_M^{ch}
(finite bias)
ΔQ
μ_M^{ch}
(zero bias)
n_e
n_h
vacuum level
right
E_c
E_v
I_h
$I_{back} = |I_e| + |I_h|$
μ_M^{ch}
(zero bias)
ΔQ
μ_M^{ch}
(finite bias)
1
2
4
FS
x
d_1
L_{sam}
d_2

Fig. 2

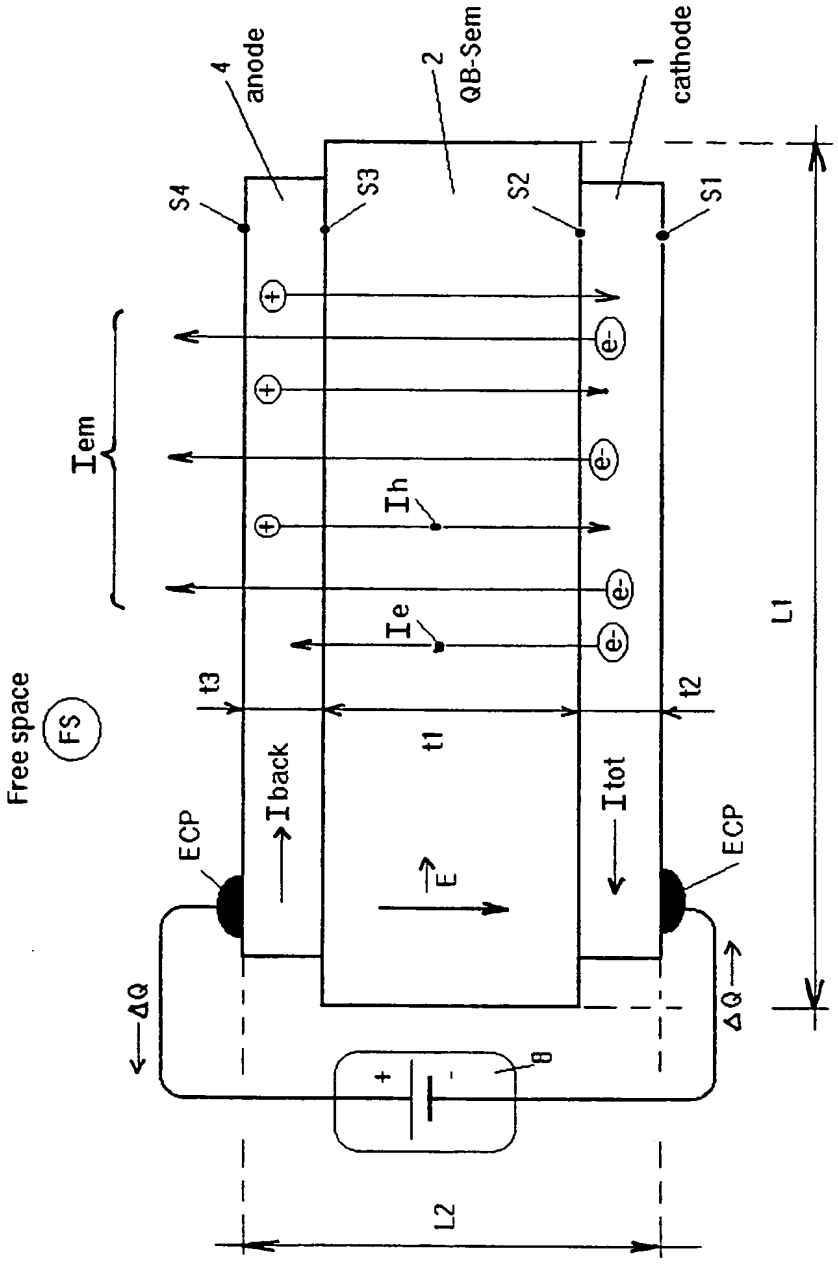
4
anode
2
QB-Sem
1
cathode
S4
S3
S2
S1
Iem
Ih
Ie
e-
Free space
FS
t3
t1
t2
L1
Iback
Itot
ECP
ECP
E
ΔQ
ΔQ
+
-
B
L2

Fig. 3

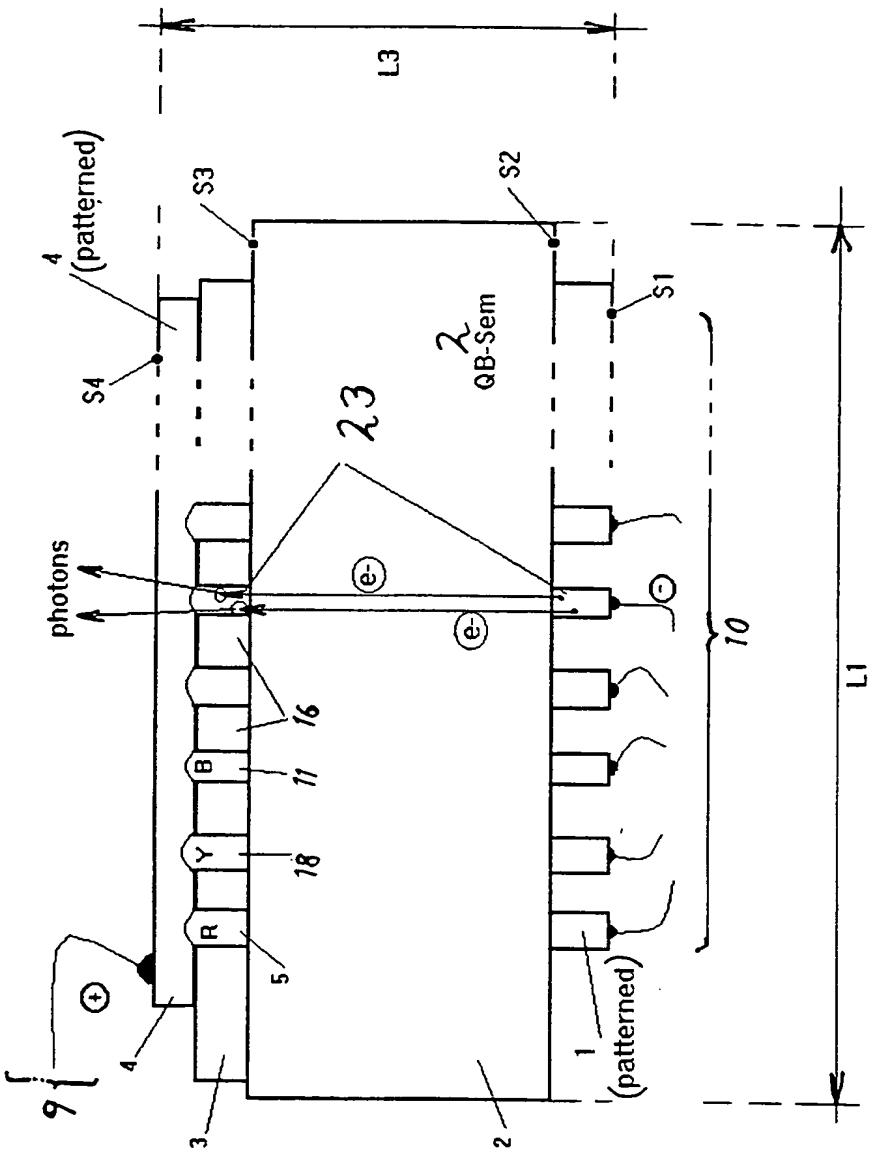
L3
L1
S1
S2
S3
S4
4 (patterned)
2 QB-Sem
23
photons
e-
e-
16
11
18
10
B
Y
R
5
4
3
2
1 (patterned)
9

Fig. 4

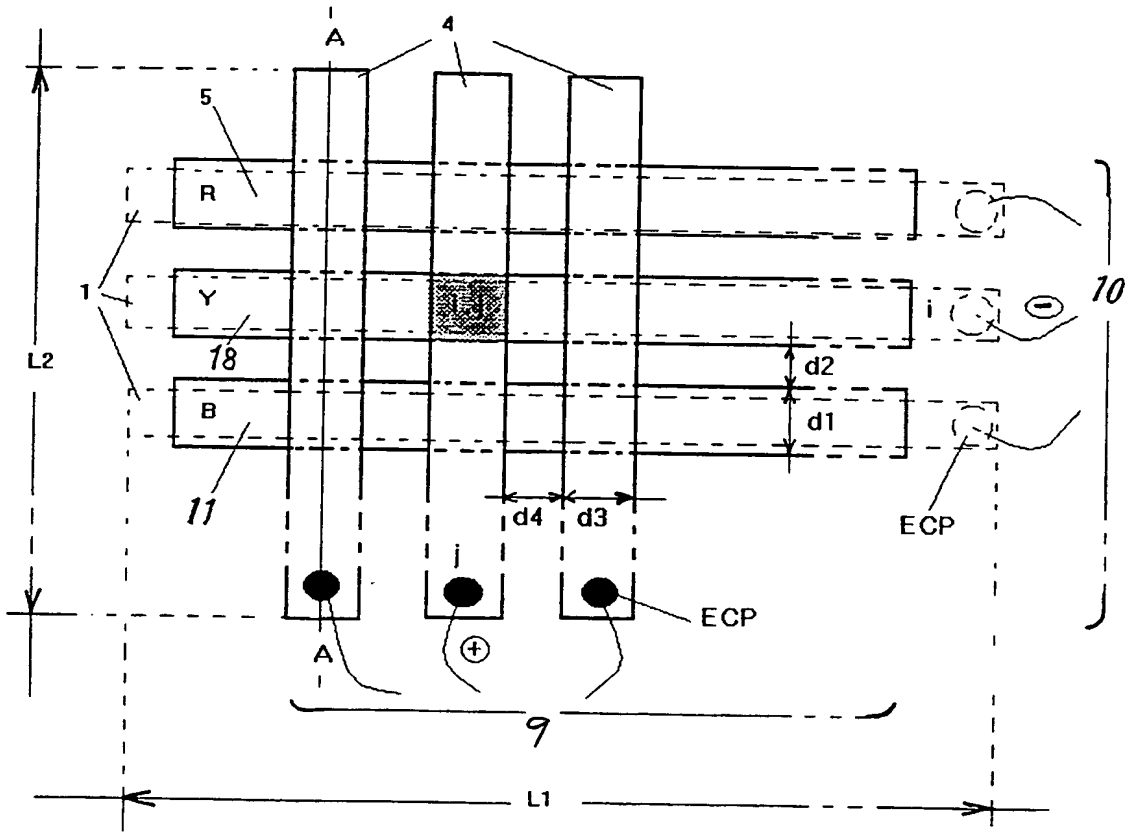

Fig. 5

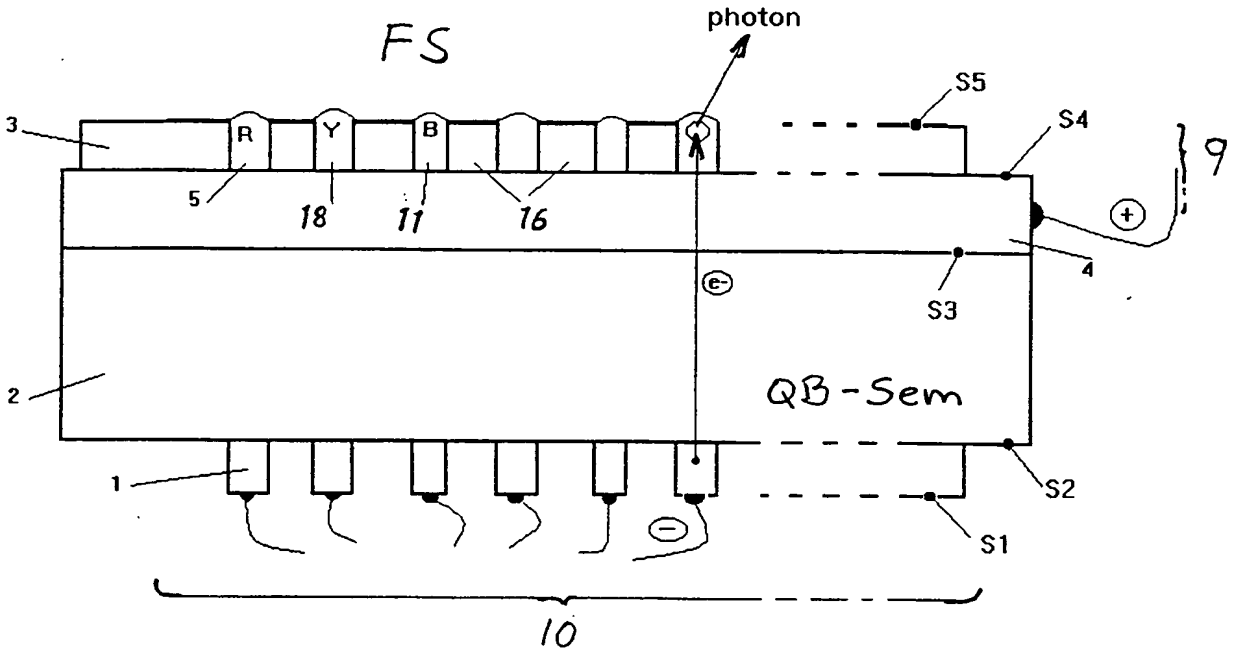

Fig. 6

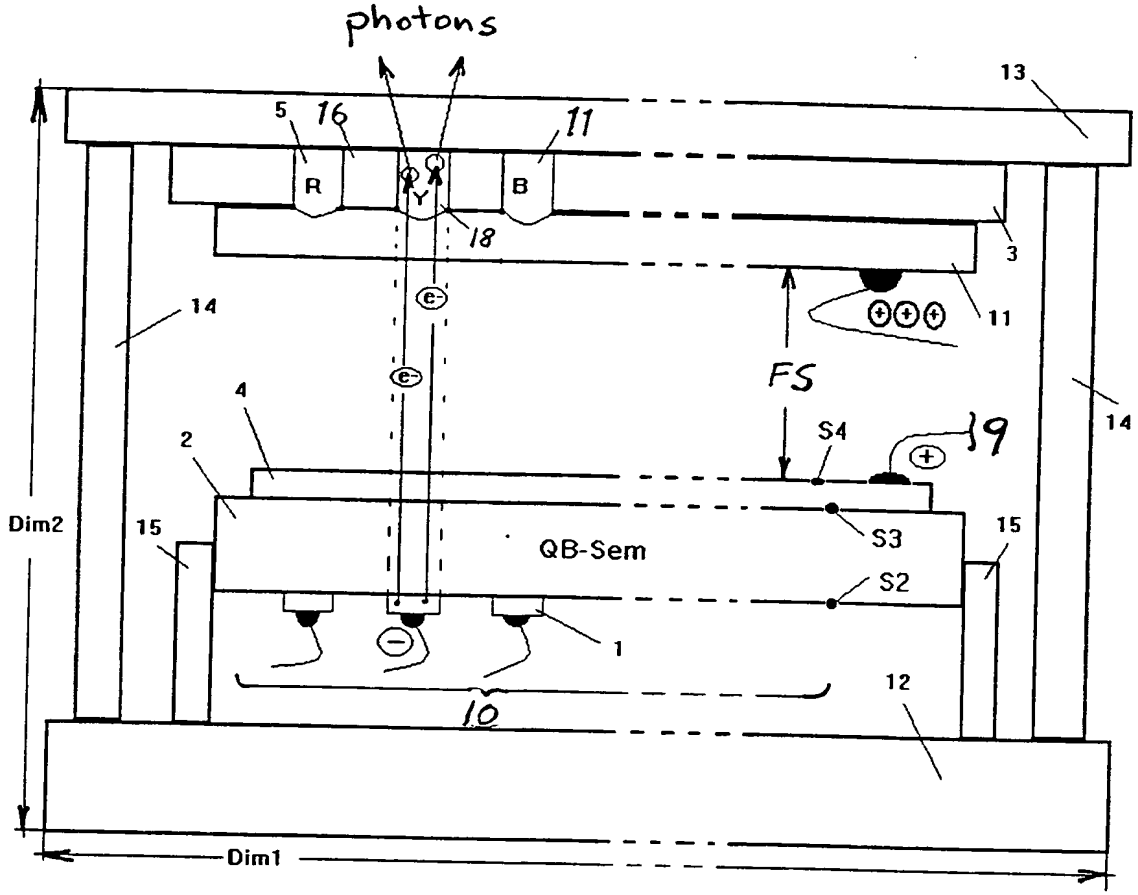
photons
13
5
16
11
R
Y
B
18
3
14
11
FS
4
2
S4
19
14
Dim2
15
QB-Sem
S3
15
S2
1
12
10
Dim1

Fig. 7

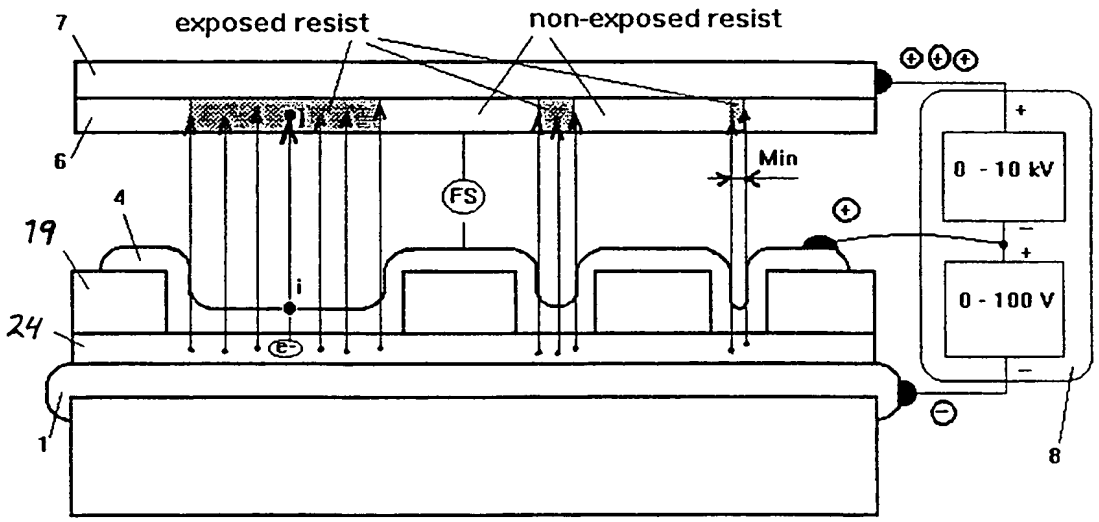
7
exposed resist
non-exposed resist
6
Min
FS
4
19
i
24
1
0 - 10 kV
0 - 100 V
8

Fig. 8

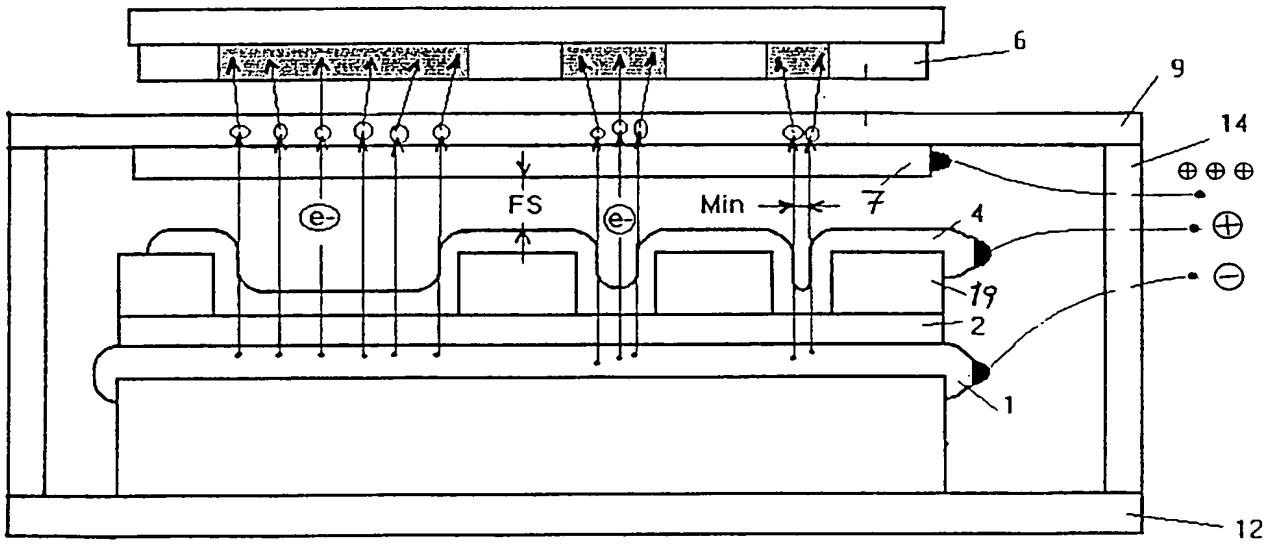

Fig. 9

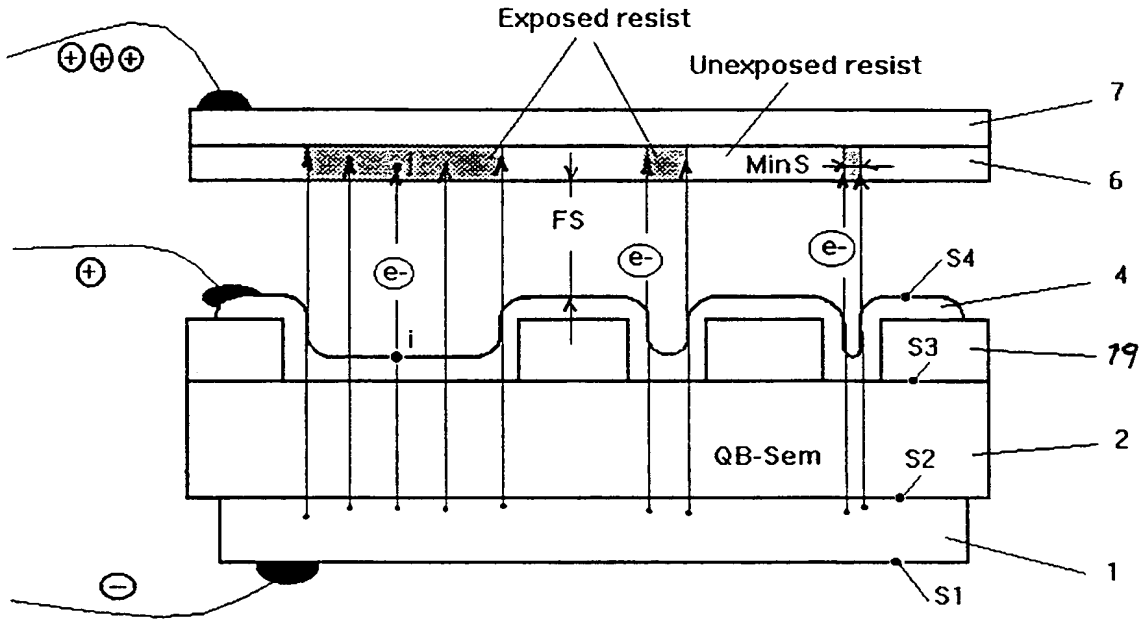
Exposed resist
Unexposed resist
7
6
MinS
FS
e-
e-
e-
S4
4
i
S3
19
QB-Sem
S2
2
1
S1

Fig. 10

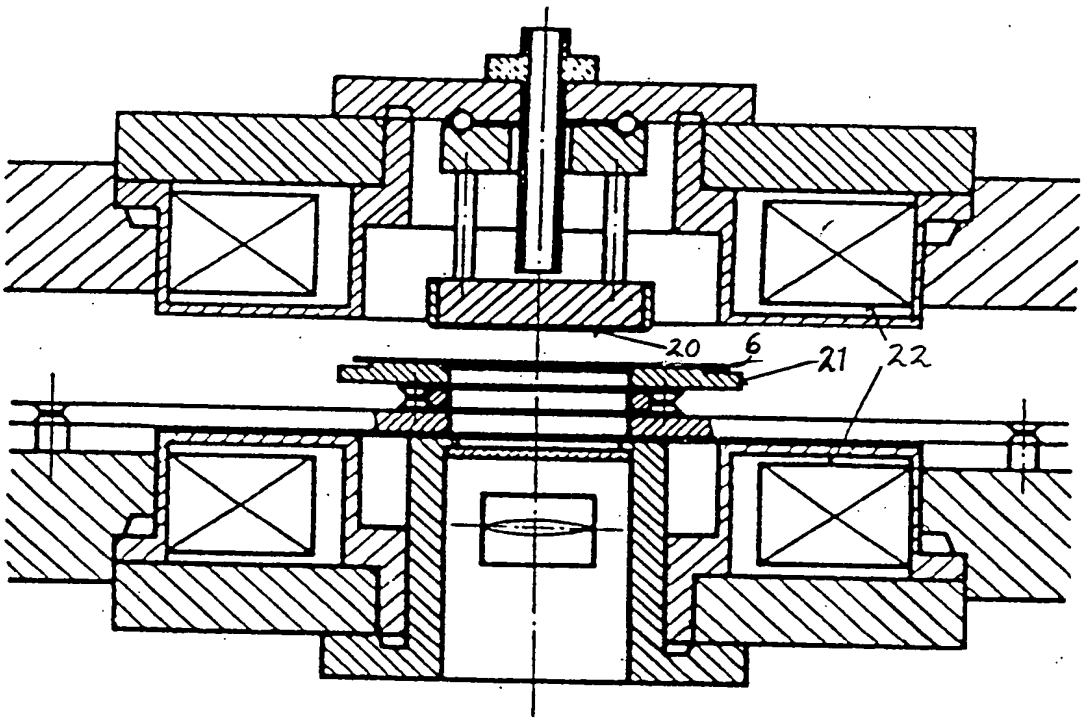

Fig. 11

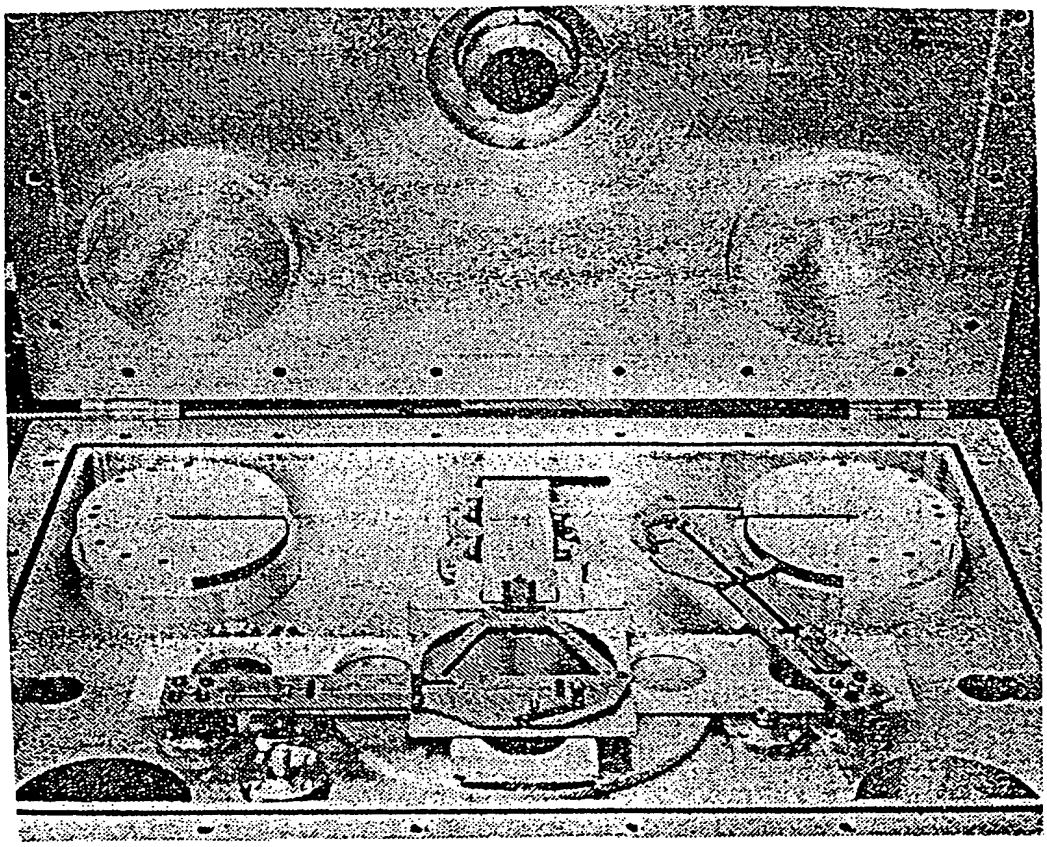

Fig. 12

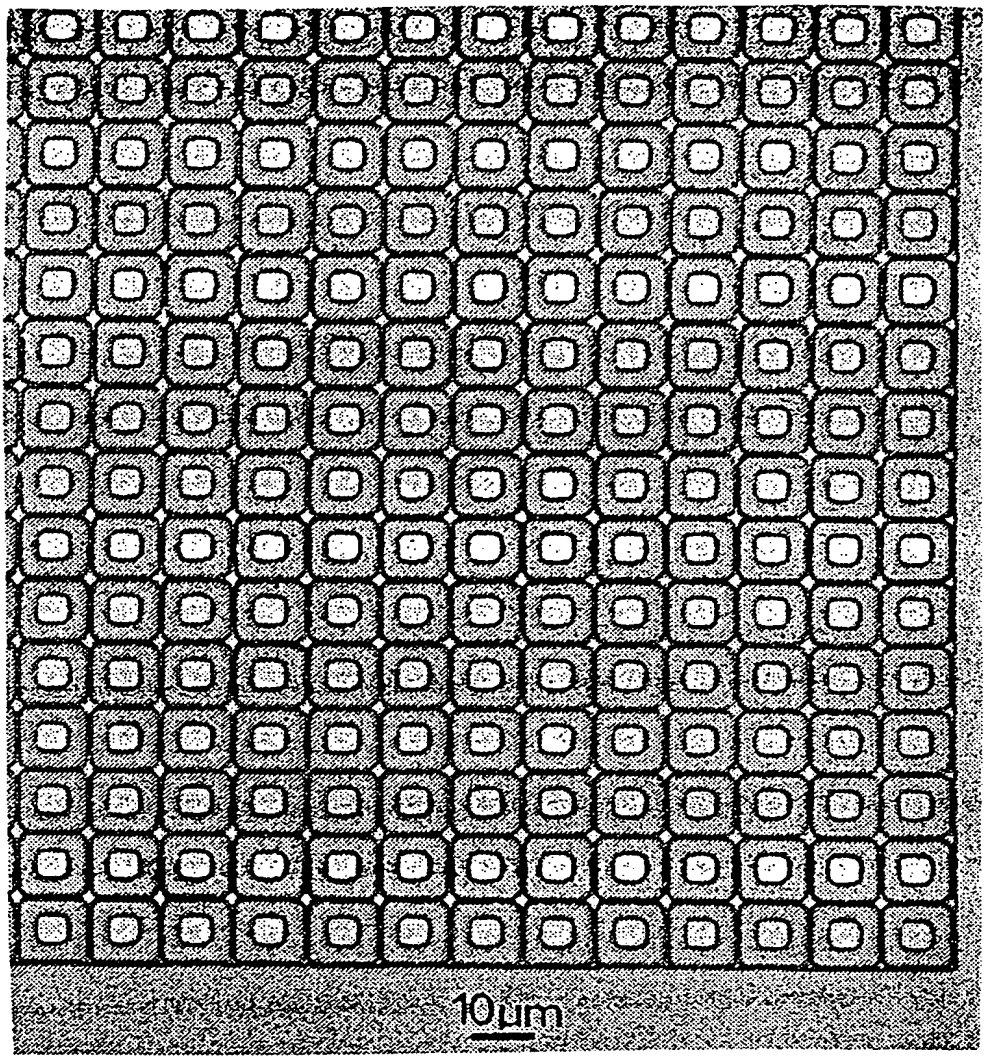

Fig. 13

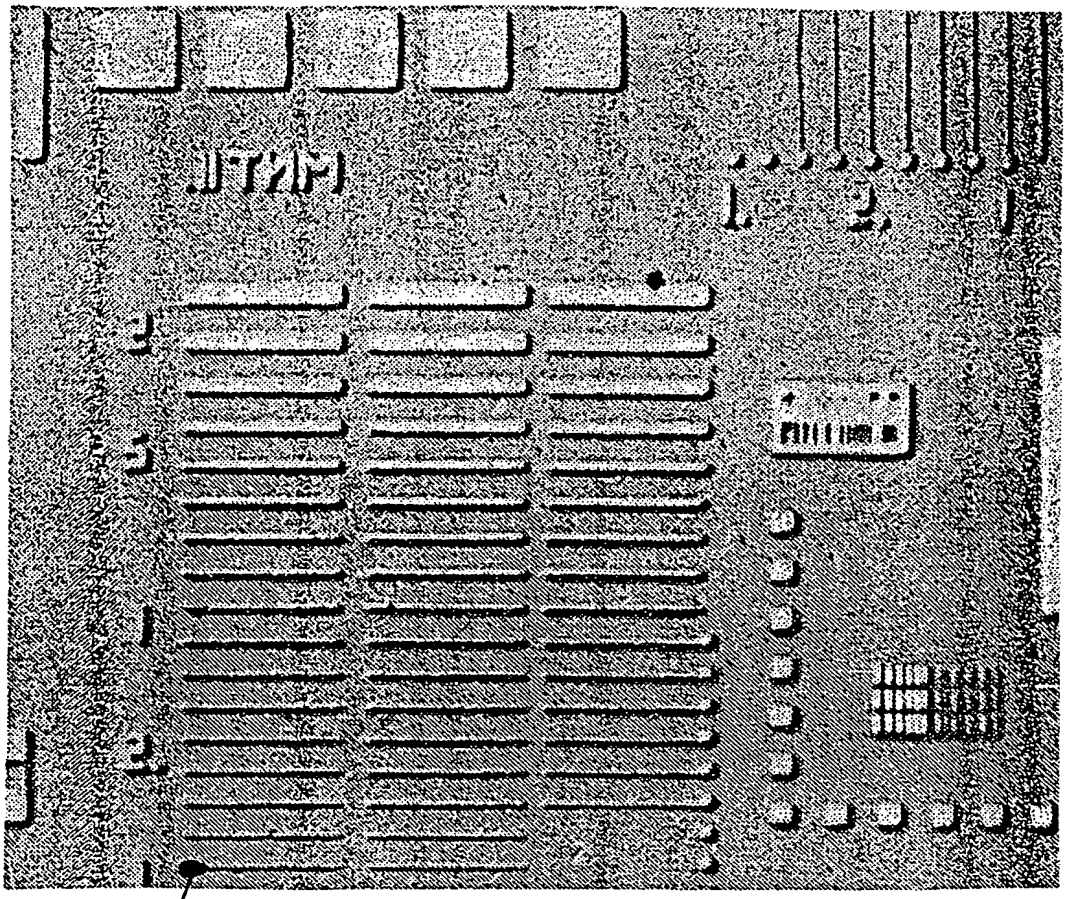

Fig. 14

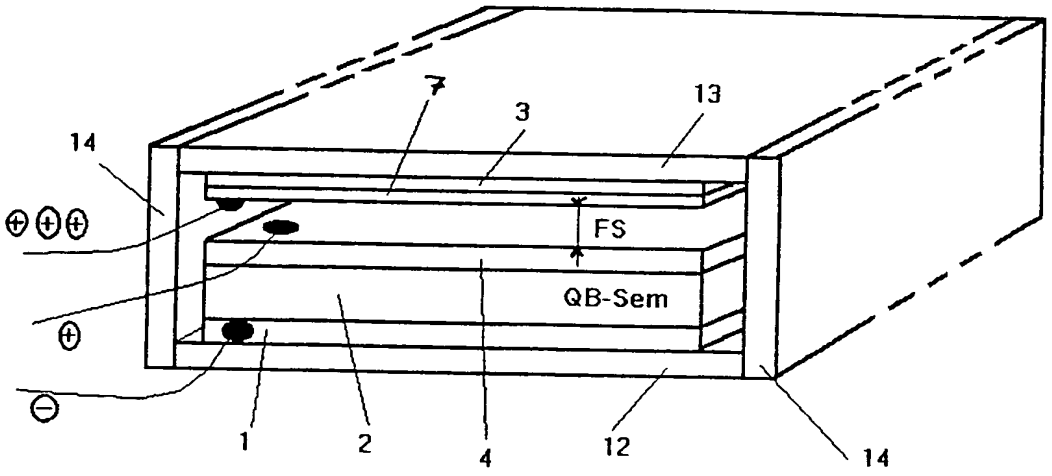

Fig. 15

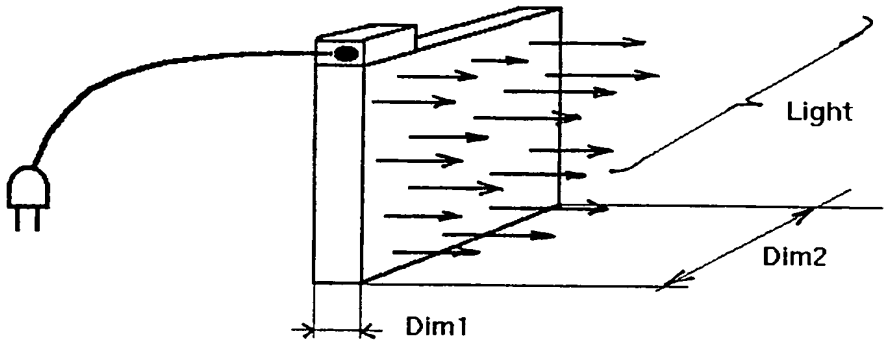

Fig. 16

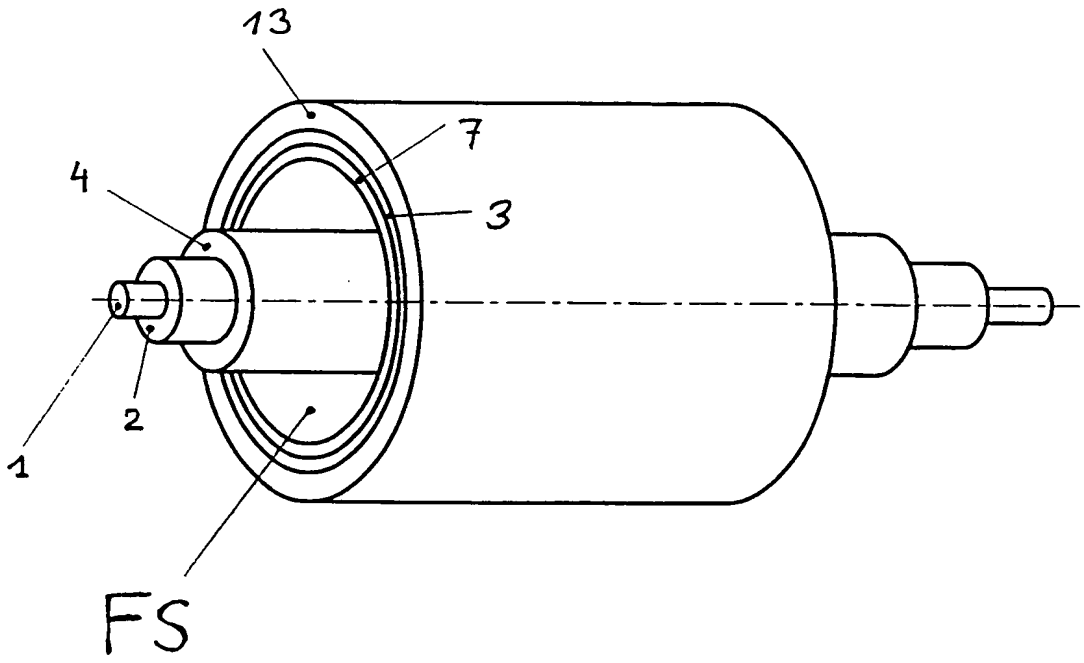

Fig. 17

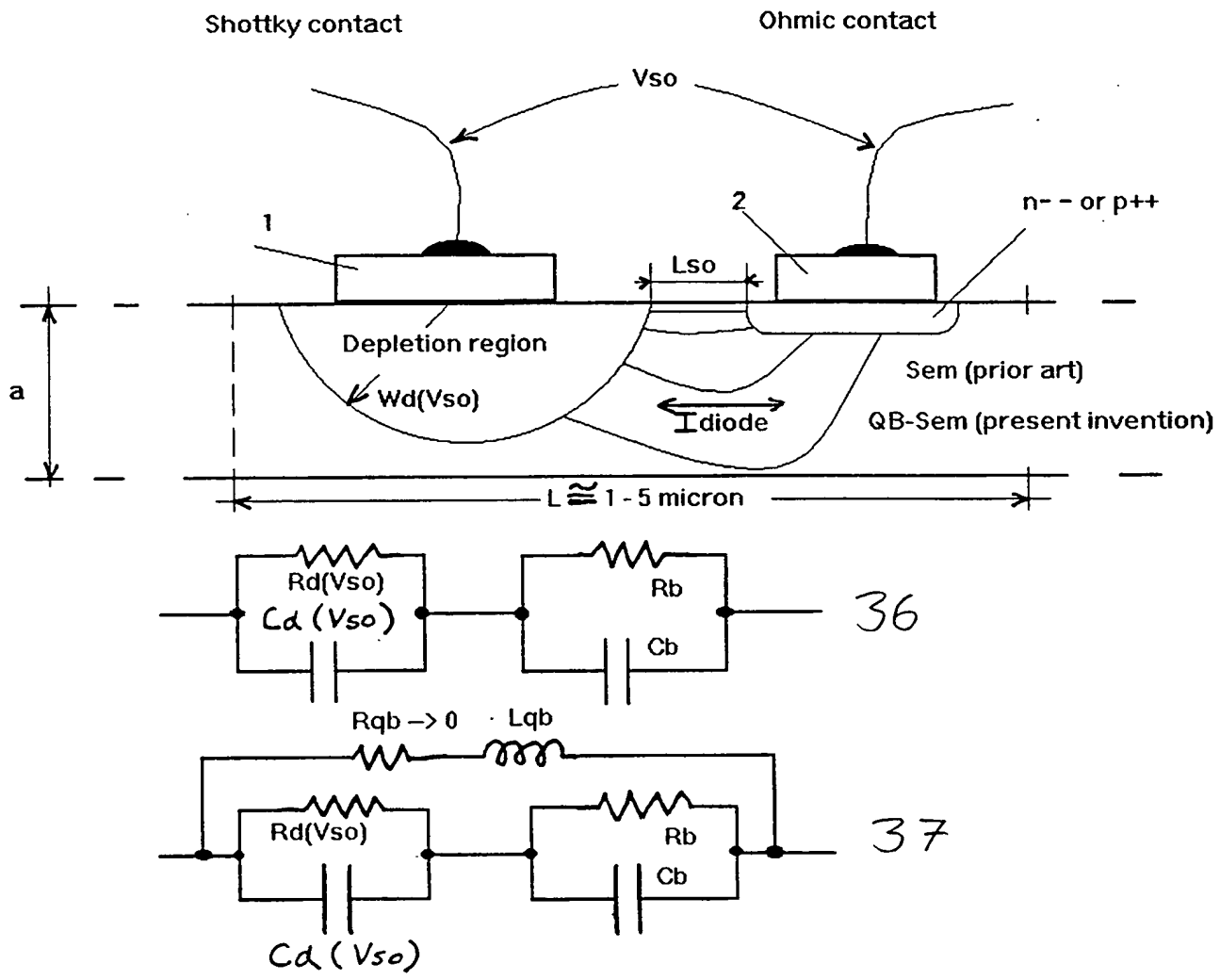
Shottky contact
Ohmic contact
Vso
1
2
n- - or p++
Lso
a
Depletion region
Wd(Vso)
Idiode
Sem (prior art)
QB-Sem (present invention)
L ≅ 1 - 5 micron
Rd(Vso)
Cd (Vso)
Rb
Cb
36
Rqb -> 0
Lqb
Rd(Vso)
Rb
Cb
37
Cd (Vso)

Fig. 18

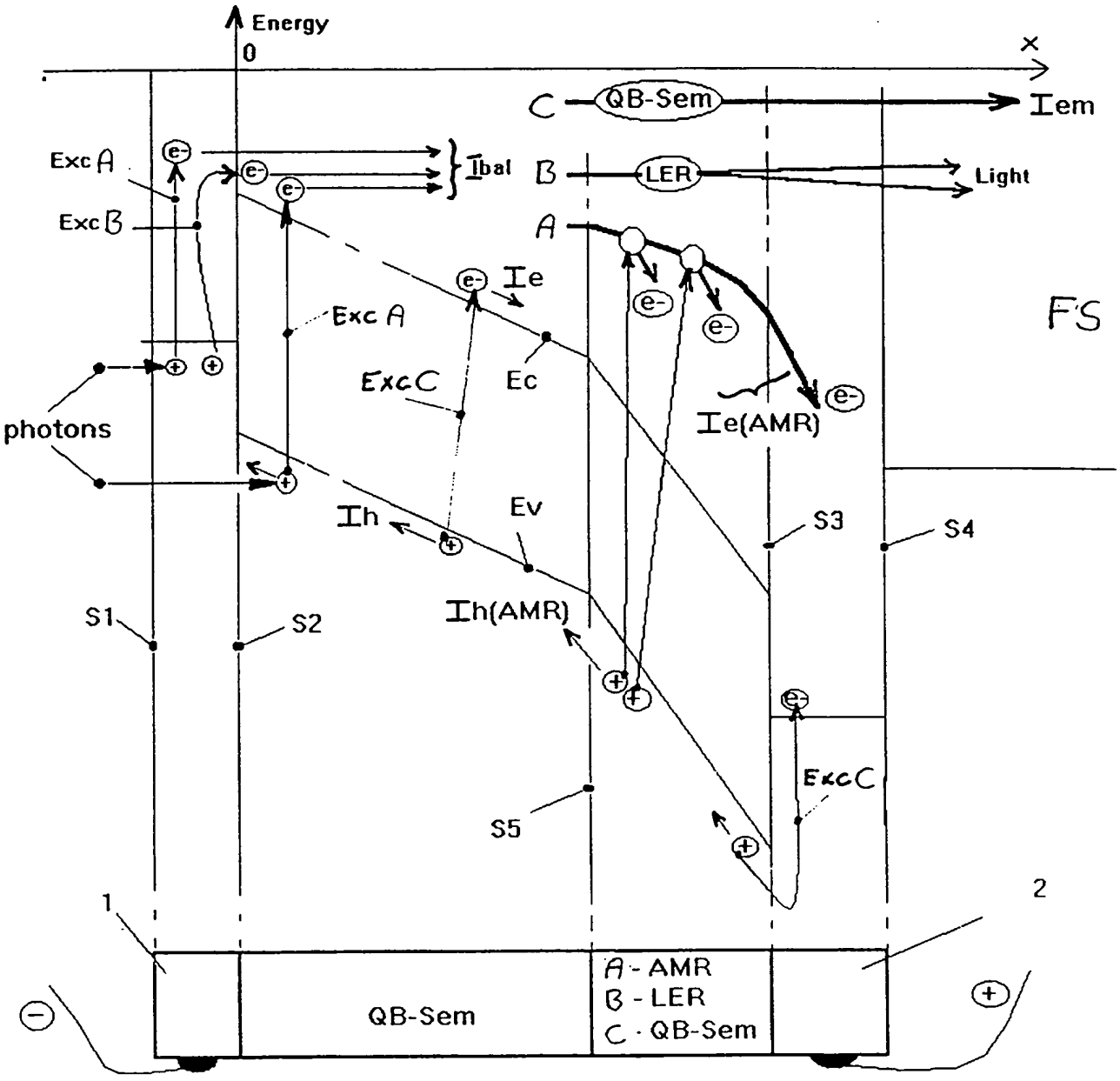
Energy
0
x
C
QB-Sem
Iem
Exc A
Ibal
B
LER
Light
Exc B
A
Ie
FS
Exc A
Exc C
Ec
photons
Ie(AMR)
Ih
Ev
S3
S4
S1
S2
Ih(AMR)
S5
Exc C
1
2
A - AMR
B - LER
C - QB-Sem
QB-Sem

Fig. 19

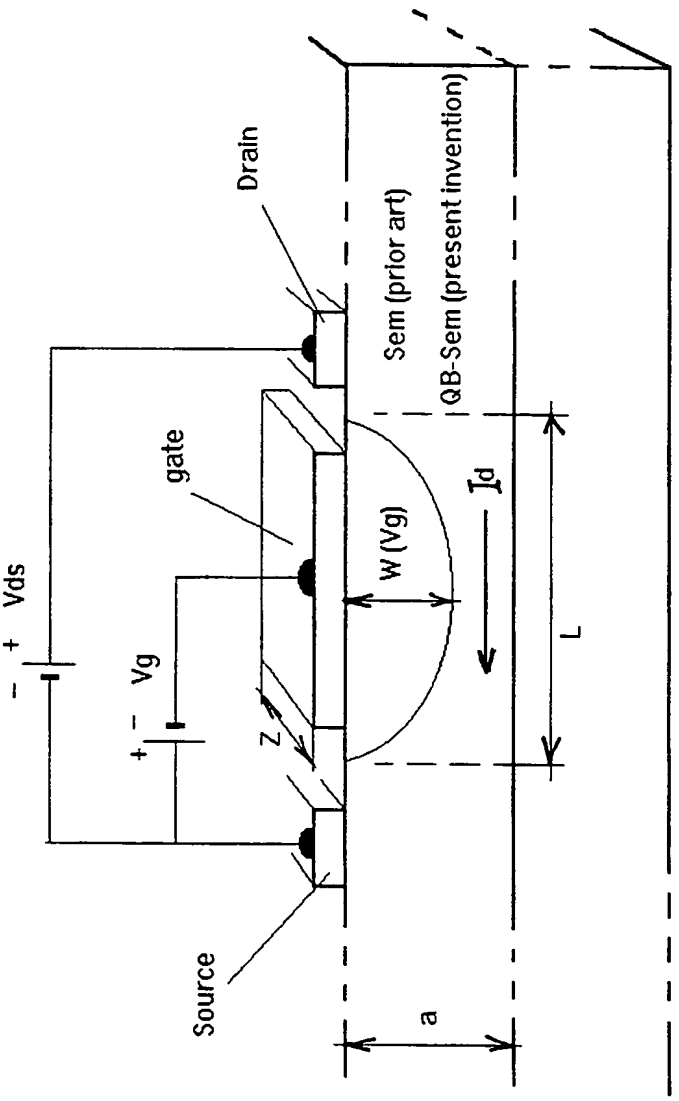
Drain
Sem (prior art)
QB-Sem (present invention)
gate
W (Vg)
Id
L
Vds
Vg
Z
Source
a

Fig. 20

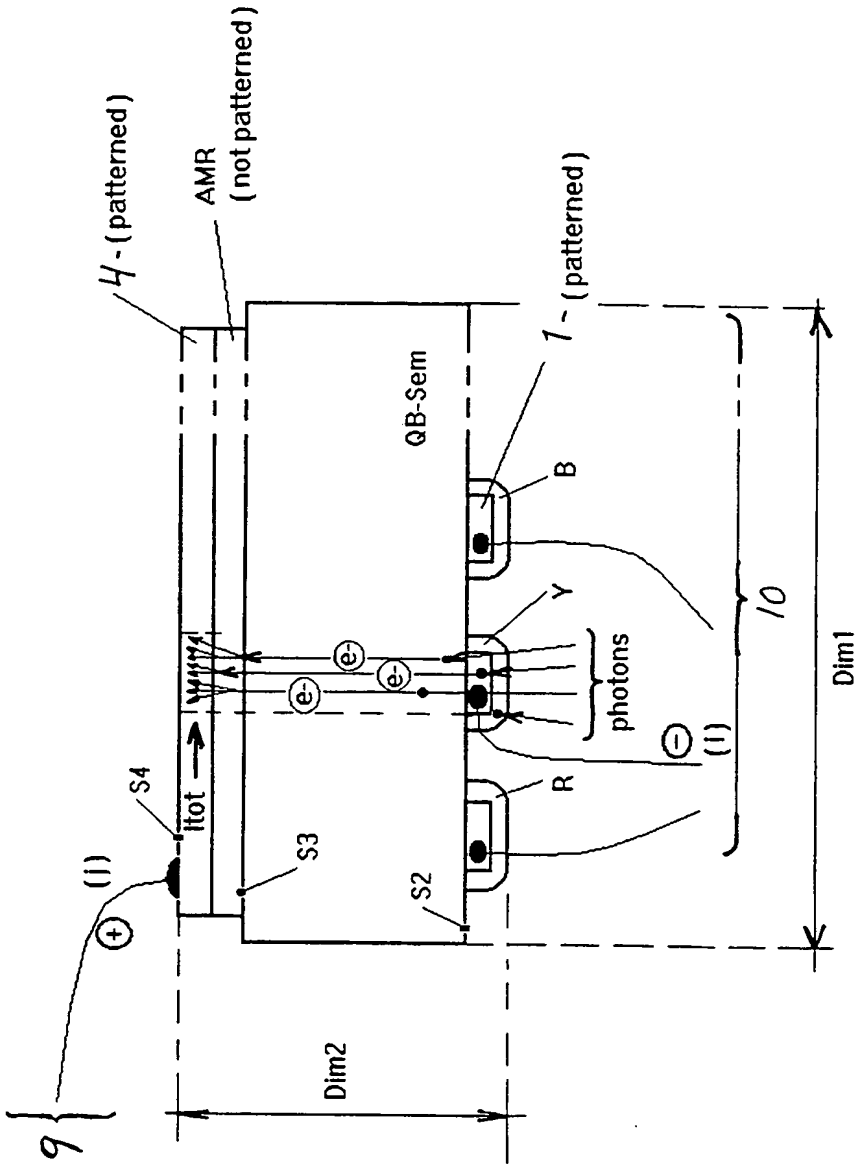
4 - (patterned)
AMR
(not patterned)
QB-Sem
1 - (patterned)
B
Y
R
photons
10
Dim1
Dim2
9
(+)
(1)
S4
S3
S2
Itot
e-
(-)

Fig. 21

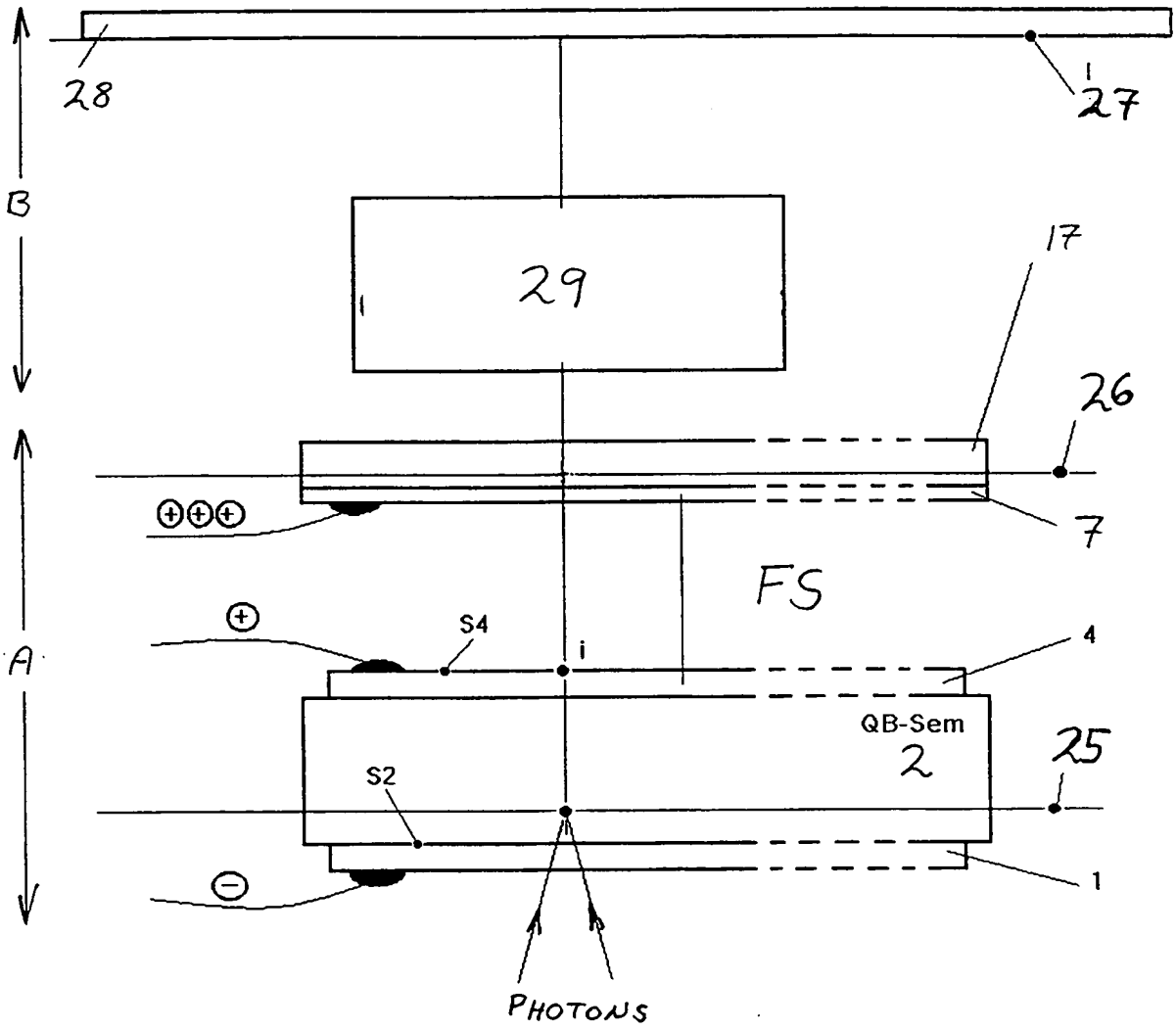

Fig. 22

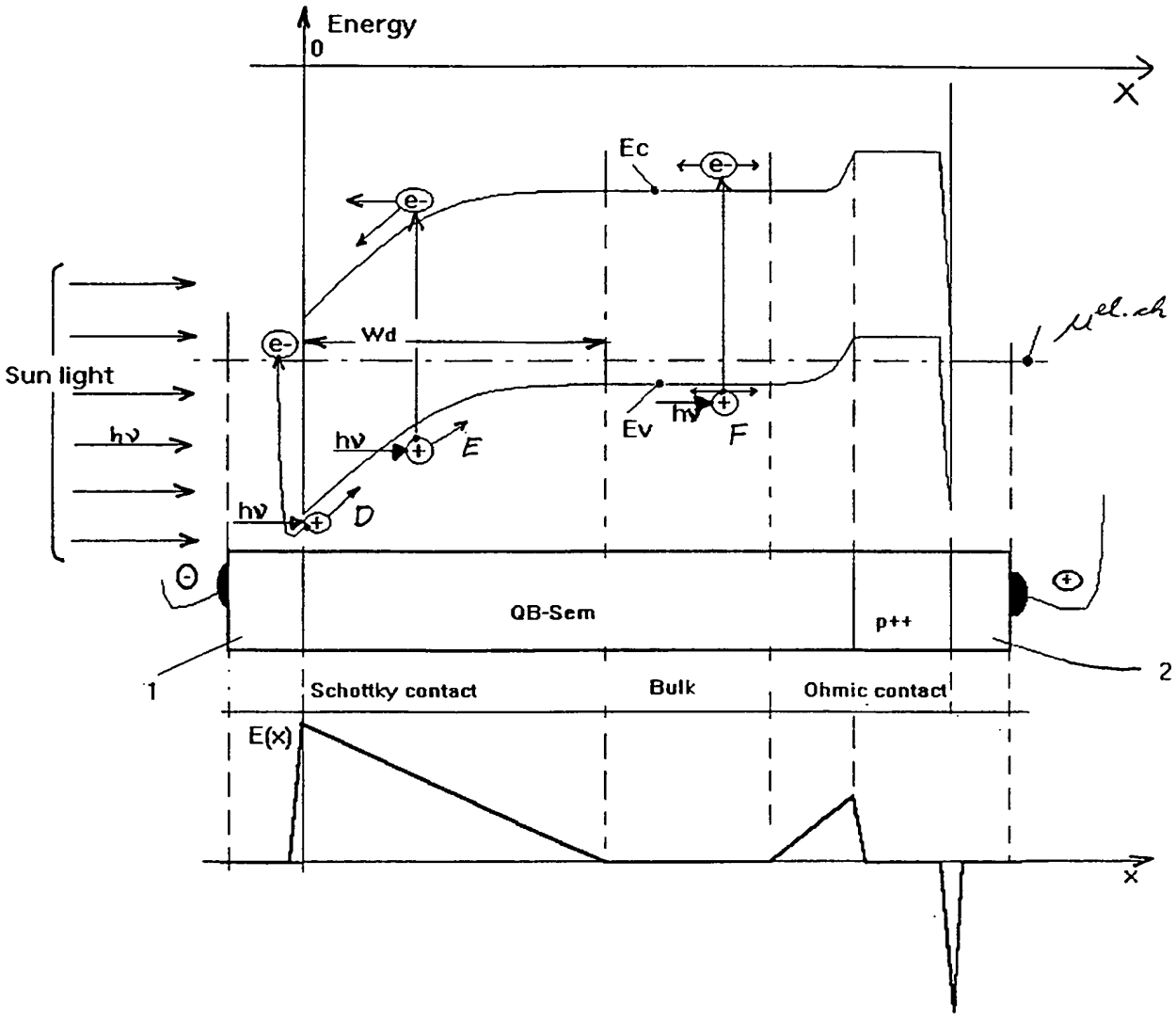
Energy
0
X
Ec
e-
Wd
Sun light
hν
E
D
Ev
F
μel.ch
QB-Sem
p++
1
2
Schottky contact
Bulk
Ohmic contact
E(x)
x

Fig. 23

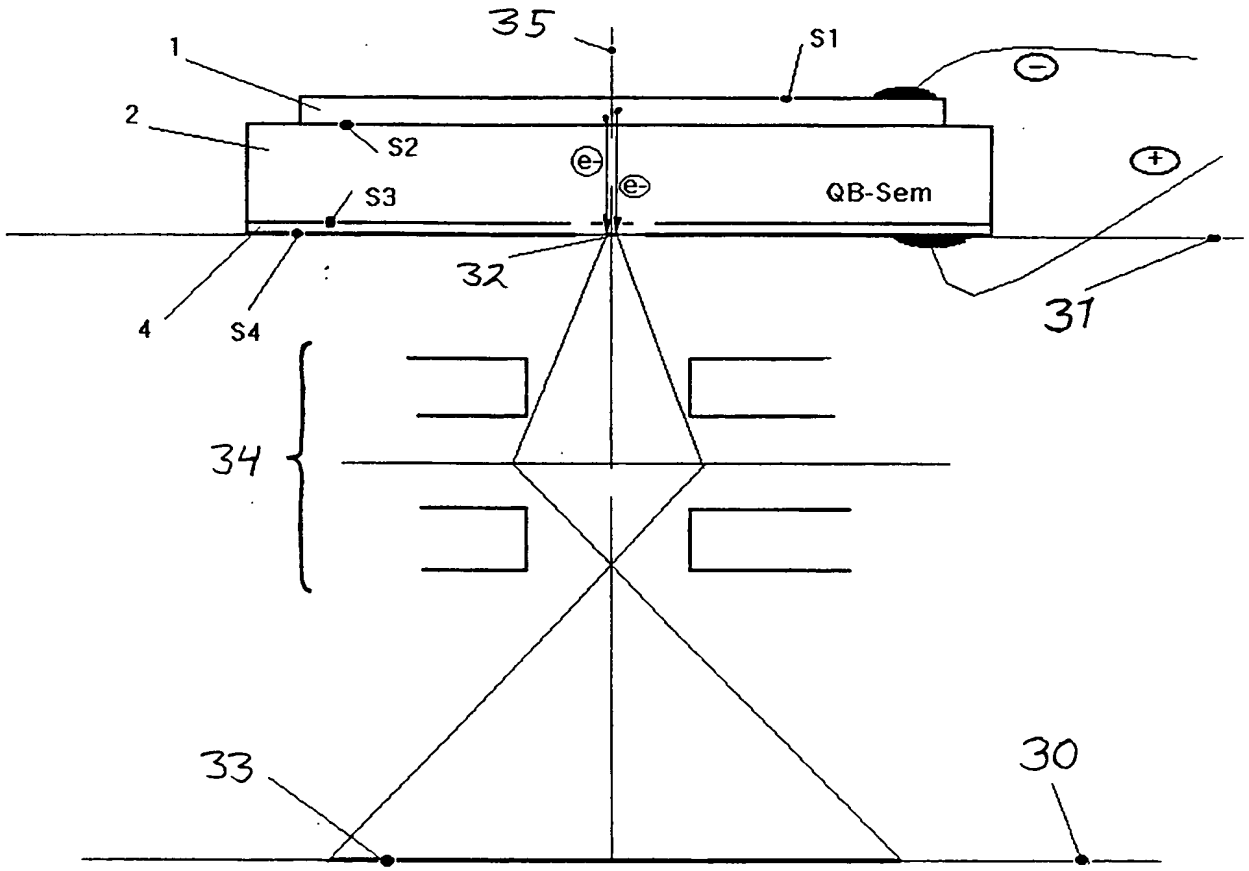

Fig. 24

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCI/DK 99/00323

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01J1/30 H01L29/76

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01J H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 1 223 729 A (NORTH AMERICAN ROCKWELL CORPORATION) 3 March 1971 (1971-03-03) page 3, line 124 - page 4, line 10 page 4, line 78 - line 77 page 4, line 110 - line 118 page 5, line 14 - line 22 page 7, line 54 - line 112 figures 2,3	1,6-10, 12,13, 18-23, 25,53, 58-62,64
Y	---	34-41, 46-52
Y	US 5 280 221 A (OKAMOTO SHINJI ET AL) 18 January 1994 (1994-01-18) figures 2A-2B	34-40

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 September 1999	28/09/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Colvin, G

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/DK 99/00323

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	DELONG A ET AL: "A 1:1 ELECTRON STEPPER" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 7, no. 6, 1 November 1989 (1989-11-01), pages 1422-1425, XP000117170 ISSN: 0734-211X the whole document	41,46-52
X	EP 0 367 195 A (MATSUSHITA ELECTRIC IND CO LTD) 9 May 1990 (1990-05-09) column 6, line 22 - line 30 column 15, line 51 - column 16, line 5 column 16, line 16 - line 40	1,13,41, 53
A	L F EASTMAN ET AL.: "Ballistic electron motion in GaAs at room temperature" ELECTRONICS LETTERS., vol. 16, no. 13, 19 June 1980 (1980-06-19), pages 524-525, XP002115049 IEE STEVENAGE., GB ISSN: 0013-5194 the whole document	2,14,26, 42,54

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/DK 99/00323

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		FR 1572047 A	20-06-1969
US 5280221 A	18-01-1994	JP 4312738 A	04-11-1992
		FR 2675306 A	16-10-1992
EP 0367195 A	09-05-1990	JP 2121227 A	09-05-1990
		JP 2126531 A	15-05-1990
		JP 2126532 A	15-05-1990
		JP 2170327 A	02-07-1990
		JP 2172127 A	03-07-1990
		US 5202605 A	13-04-1993